## GENERAL DESCRIPTION

OB3392K is an offline LED lighting controller with primary side control, high power factor and high constant current (CC) precision, which can achieve low system cost for an isolated lighting application in a single stage converter. It significantly simplifies the LED lighting system design by eliminating the secondary side feedback components and the opto-coupler.

The proprietary CC control scheme is used and the system can achieve high power factor with constant on-time control scheme. Quasi-resonant (QR) operation and clamping frequency greatly improves the system efficiency. The constant output current is compensated for tolerance of transformer inductance variation. And the line compensation and load compensation are built in OB3392K for high precisely constant output current control.

OB3392K offers comprehensive protection coverage with auto-recovery features including LED open loop protection, LED short circuit protection, cycle-by-cycle current limiting, built-in leading edge blanking, VDD under voltage lockout (UVLO), etc.

OB3392K is offered in SOT23-6 package.

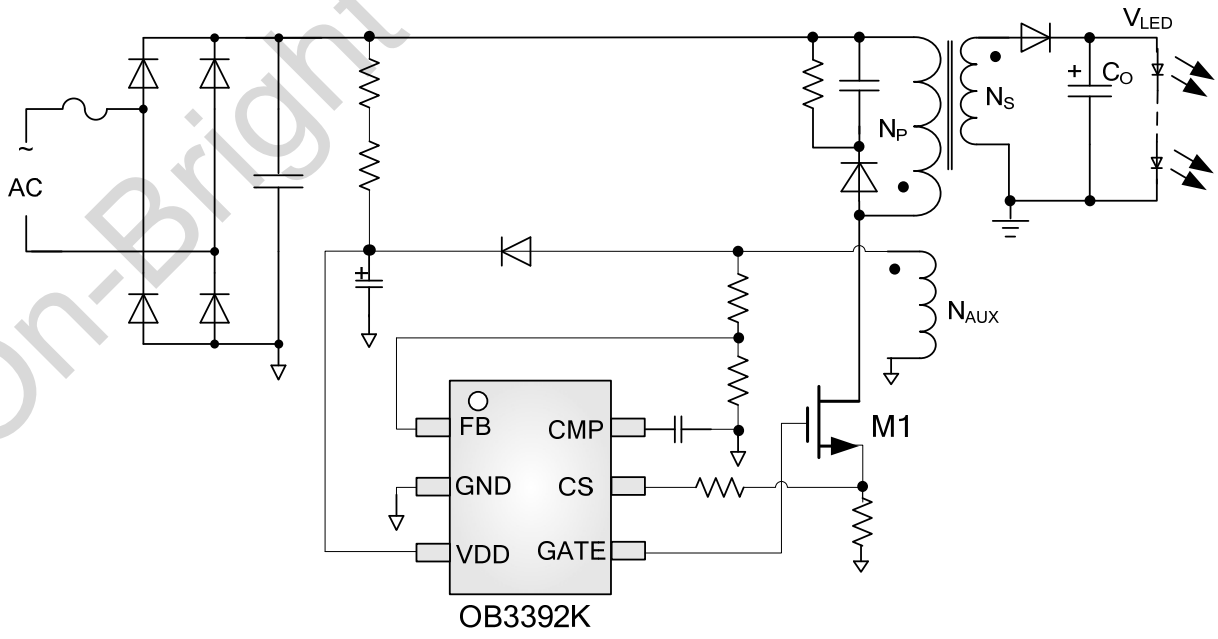
## FEATURES

- High power factor
- High precision constant current regulation at universal AC input
- Primary-side sensing and regulation without TL431 and opto-coupler
- Low system cost and high efficiency
- Quasi-resonant operation
- Programmable CC regulation
- Built-in primary winding inductance compensation
- Built-in line compensation
- Built-in load compensation
- LED short circuit protection
- LED open loop protection
- Cycle-by-cycle current limiting
- Built-in leading edge blanking (LEB)
- VDD under voltage lockout with hysteresis
- VDD over voltage protection
- Over temperature protection (OTP)

## APPLICATIONS

- LED lighting

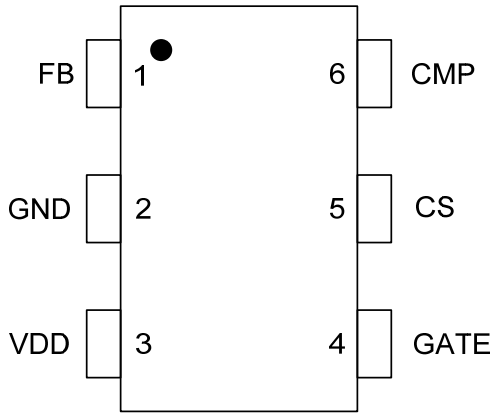
## TYPICAL APPLICATION



## GENERAL INFORMATION

### Pin Configuration

The pin map is shown as below for SOT23-6.




### Ordering Information

| Part Number | Description |
|---|---|
| OB3392KMP | SOT23-6, Pb-free, T&R |

**Note:** All Devices are offered in Pb-free Package if not otherwise noted.

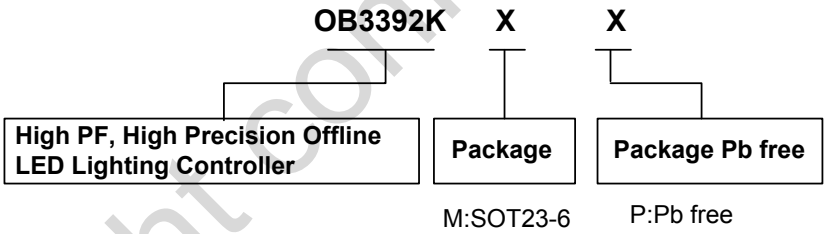
### Package Dissipation Rating

| Package | RθJA (℃/W) |
|---|---|
| SOT23-6 | 200 |

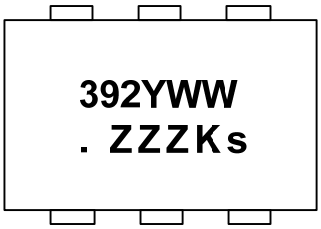
### Absolute Maximum Ratings

| Parameter | Value |
|---|---|
| VDD Voltage | -0.3 to 40V |
| Gate Voltage | -0.3 to 13V |
| CS Input Voltage | -0.3 to 7V |
| FB Input Voltage | -0.3 to 7V |
| COMP Voltage | -0.3 to 7V |
| Min/Max Operating Junction Temperature $T_J$ | -40 to 150 ℃ |
| Min/Max Storage Temperature $T_{stg}$ | -55 to 150 ℃ |
| Lead Temperature (Soldering, 10secs) | 260 ℃ |

**Note:** Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



## Marking Information

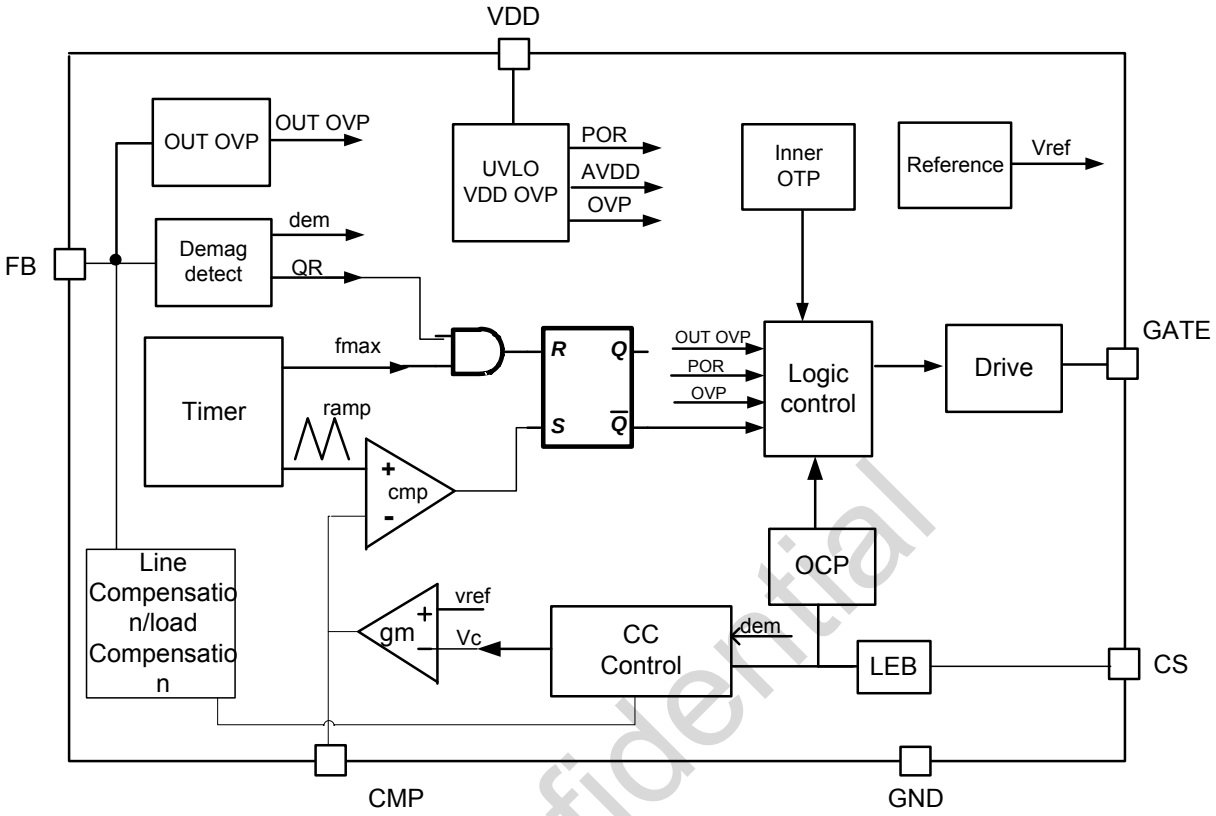



Y:Year Code
WW:Week Code(01-52)
ZZZ: Lot code
K:Character Code
s: Internal code

## TERMINAL ASSIGNMENTS

| Pin Num | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | FB | I | Voltage feedback from auxiliary winding. Connected to resistor divider from auxiliary winding reflecting output voltage. |
| 2 | GND | P | Power Ground. |
| 3 | VDD | P | Power supply Input. |
| 4 | GATE | O | Gate driver output for power MOSFET. |
| 5 | CS | I | Current sensing terminal. |
| 6 | CMP | O | Loop compensation pin. A capacitor is connected between CMP and GND. |

## BLOCK DIAGRAM

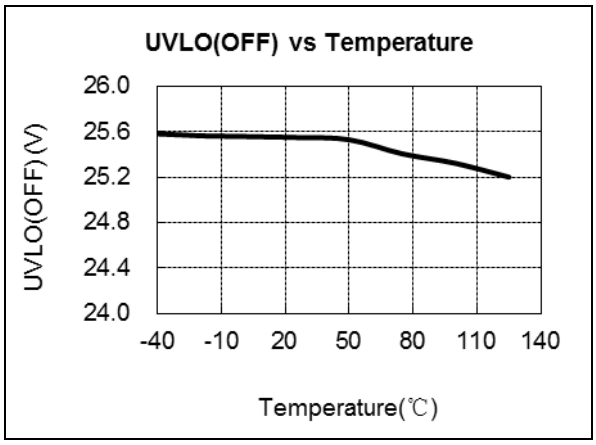


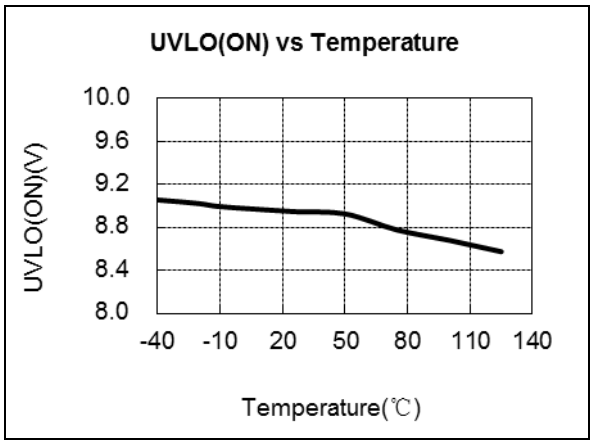
## ELECTRICAL CHARACTERISTICS

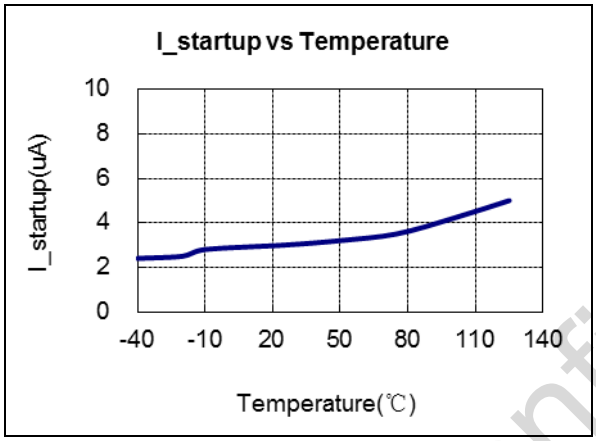
(TA = 25℃, VDD=20V, if not otherwise noted)

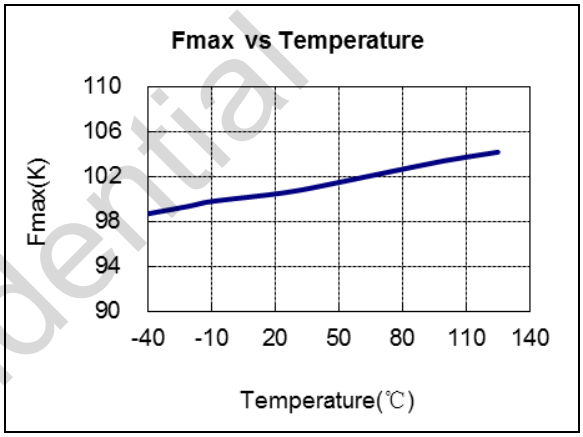
| Symbol | Parameter | Test Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply Voltage (VDD) Section** | | | | | | |
| $I_{start-up}$ | Start up current | VDD=UVLO(OFF)-1V | | 3 | 7 | uA |
| $I_{op}$ | Operation current | VDD=20V, no loading | | 1.5 | 2.2 | mA |
| UVLO(OFF) | VDD under voltage lockout exit | | 24 | 25.5 | 27 | V |
| UVLO(ON) | VDD under voltage lockout enter | | 8 | 9 | 10 | V |
| VDD_OVP | VDD Over Voltage Protection | | 32 | 35 | 38 | V |
| **Current Sense Input Section** | | | | | | |
| TLEB | LEB time | | | 0.3 | | us |
| Vth_ocp | Over Current Threshold | FB>0.45V | 0.95 | 1.00 | 1.05 | V |
| | | FB<0.45V | | 0.5 | | V |
| **FB Input Section** | | | | | | |
| Vout_ovp | Output Over Voltage Protection | | 3.4 | 3.5 | 3.6 | V |
| Vout_scp | Output Short Circuit Protection | | | 0.45 | | V |
| **QR Section** | | | | | | |
| Fmax | Maximum Working Frequency | | | 100 | | KHz |
| Toff_max | Maximum Off Time | CMP=4.2V | | 70 | | us |
| Toff_min | Minimum Off Time | CS>0.15V | | 2 | | us |
| | | CS<=0.15V | | 0.5 | | us |
| Ton_max | Maximum On Time | CMP=4.2V | | 25 | | us |
| **Error Amplifier Section** | | | | | | |
| Vref | Error Amplifier Reference Voltage | | 0.196 | 0.200 | 0.204 | V |
| Gm | Error Amplifier Transconductance | | | 50 | | us |
| Isource_max | Error Amplifier Maximum Source Current | | | 10 | | uA |
| Isink_max | Error Amplifier Maximum Sink Current | | | 50 | | uA |
| Vclamp_cmp | CMP Pin Down_clamp Voltage | | | 1.2 | | V |
| **Gate Driver Section** | | | | | | |
| Vol | Output Low Level | Iout=10mA | | | 1 | V |
| Voh | Output High Level | Iout=10mA | 6 | | | V |
| Vclamp | Output Up-Clamping Voltage | | | 12 | | V |
| Tr | Rising Edge Time | Cl=1nF | | 110 | | ns |
| Tf | Falling Edge Time | Cl=1nF | | 70 | | ns |

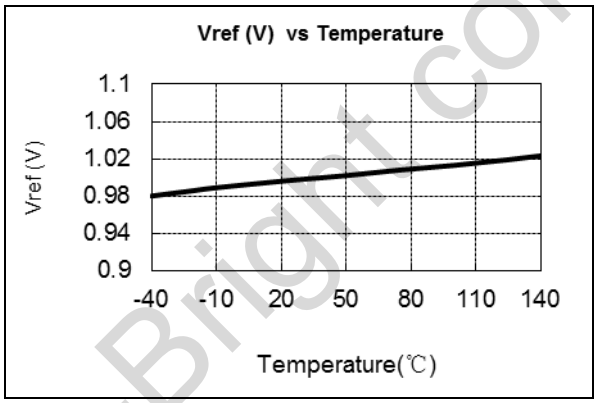
## CHARACTERIZATION PLOTS

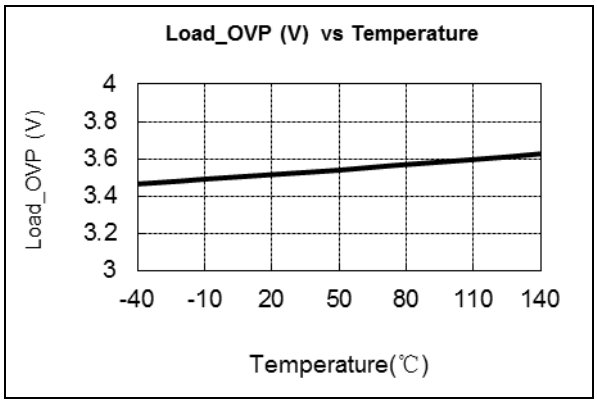


## OPERATION DESCRIPTION

OB3392K is a primary-side-control and high power factor fly-back PWM controller specialized for LED lighting application. It operates in primary side sensing and regulation, thus opto-coupler and TL431 are not required. OB3392K works at Quasi-Resonant operation with maximum working frequency clamping, which can improve the efficiency of LED lighting system design.

- **Start up Control**

Low start-up current is designed in OB3392K so that VDD could be charged up above UVLO threshold with small charging current. A large value startup resistor can therefore be used to minimize the power loss in application.

The capacitor at CMP pin is pulled up quickly during starting up until its voltage reaches 1.2V. Then the error amplifier charges the CMP pin capacitor with a transconductance of about 500uS (typical), and the Gate drives external power MOSFET at minimum frequency for low power dissipation. At the startup, the threshold voltage of OCP is set at 0.5V (typical). When the voltage at FB pin reaches 0.45V (typical), the threshold voltage of OCP is increased to 1V (typical). When the voltage at FB pin increases and reaches 1.2V (typical), the transconductance of error amplifier is reduced to 50uS (typical).

- **LED Constant Current Regulation**

The LED output current equals to the average of the output rectifier diode current. So the LED output current is related with the transformer peak current value and the transformer current discharge time. The transformer current discharge time is sensed through FB pin and the transformer peak current value is determined by internal reference voltage. A proprietary CC control block calculates LED output current through the CS pin peak current value and the transformer current discharge time. The output of the calculation is compared with an internal precise reference to generate an error voltage (Vcmp), which determines the turn-on time in voltage mode control. The LED output current can be approximated as:

$$I_{LED} = \eta \cdot \frac{N}{2} \cdot \frac{Vref}{R_{CS}}$$

$\eta$ — The transformer coupling coefficient.

N — Turn ratio of primary side winding to secondary side winding.

Rcs — The sensing resistor connected between the MOSFET source and GND.

Vref — Internal reference voltage.

- **PFC and THD**

The duration of the turn on period ton is generated by comparing an internal fixed saw-tooth wave with the voltage on the CMP pin. During steady state operation, the voltage on the CMP pin Vcmp is slowly varying due to a large external capacitor connected at the CMP pin, therefore the turn on time ton is constant. In a fly-back topology, constant turn on time and quasi-resonant operation provide high power factor (PF) and low total harmonic distortion (THD).

- **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting (OCP) is offered in OB3392K. The switching current is detected by a sense resistor connected between the CS pin and GND. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to snubber diode reverse recovery so that the external RC filter is no longer required. The current limit comparator is disabled at this blanking time and thus the external MOSFET cannot be turned off during this blanking time.

- **Quasi-Resonant Operation**

OB3392K performs quasi-resonant detection through FB pin by monitoring the voltage activity on the auxiliary windings in series with external resistors. When the stored energy of fly-back transformer is fully released to the output, the voltage at FB pin decreases. When FB pin voltage falls below 0.1V (typical), an internal FB comparator is triggered and a new PWM switching cycle is initiated following the FB triggering.

- **Line/Load Compensation**

OB3392K provides internal line compensation and load compensation to avoid using outside sensing devices. The compensated voltage is added to CS voltage cycle-by-cycle and LED output current is kept constant under different line voltage and output voltage.

- **Output OVP Protection**

An output over-voltage condition is monitored independently by the voltage at pins FB. During normal operation, when the voltage at FB pin exceeds a threshold of approximately 3.5V (typical), the over-voltage protection function is activated and the GATE is turned off immediately until VDD voltage drops below UVLO (ON), and the device enters power on startup sequence thereafter.

- **VDD Over Voltage Protection**

VDD is supplied with transformer auxiliary winding output. When VDD is higher than 35V (typical), VDD OVP protection is triggered and GATE is shut

down, and the device enters power on startup sequence thereafter.

- **LED Short Circuit Protection**

When LED string is short, the positive plateau of auxiliary winding voltage is also near zero and the FB voltage is low. If the voltage at FB pin is lower than a threshold of approximately 0.45V (typical), the IC will work at minimum frequency and the threshold voltage of OCP is reduced to 0.5V (typical). The power dissipation is greatly reduced in this way.

- **LED Open Circuit Protection**

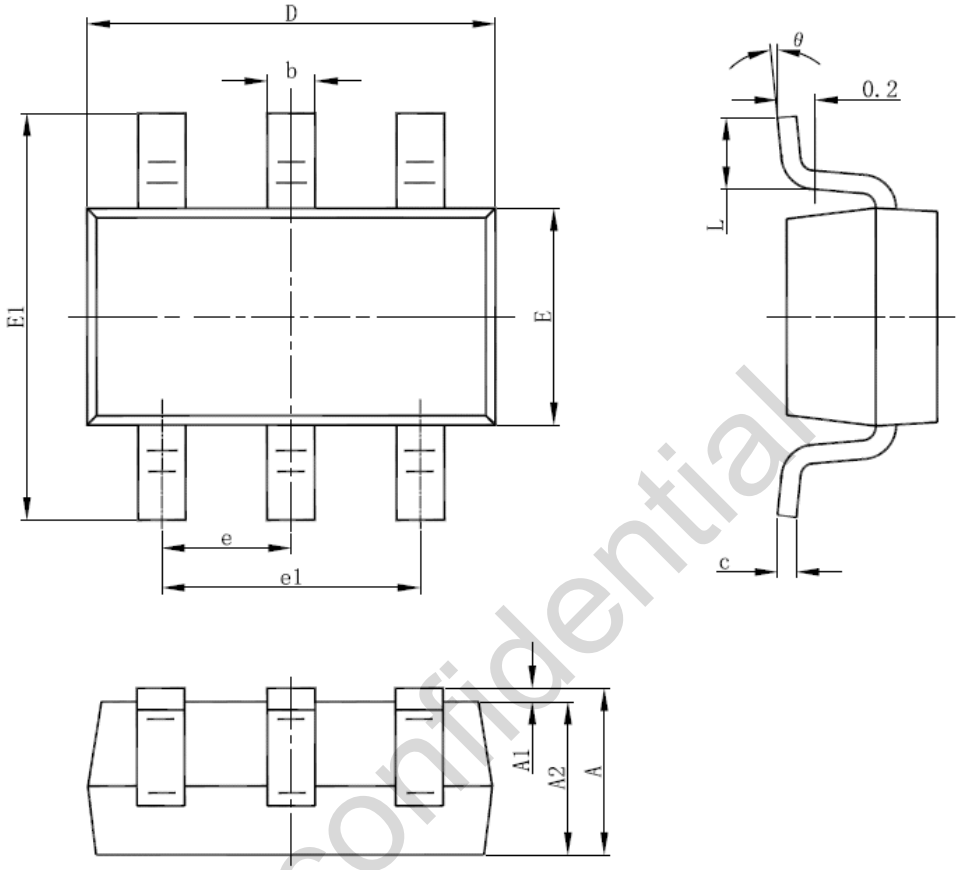
When the LED string open circuit happens, the positive plateau of auxiliary winding voltage increases and the FB pin voltage is high. If the voltage at FB pin is higher than a threshold of approximately 3.5V (typical), the IC will shut down and enter power on startup sequence thereafter.

- **Gate Driver**

The GATE pin is connected to the gate of an external power switch. An internal 12V (typical) clamp is added for MOSFET gate protection at high VDD voltage. When VDD voltage drops below UVLO(ON), the GATE pin is internally pulled low to maintain the off state.

## PACKAGE MECHANICAL DATA

### SOT-23-6L PACKAGE OUTLINE DIMENSIONS




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.000 | 1.450 | 0.039 | 0.057 |
| A1 | 0.000 | 0.150 | 0.000 | 0.006 |
| A2 | 0.900 | 1.300 | 0.035 | 0.051 |
| b | 0.300 | 0.500 | 0.012 | 0.020 |
| c | 0.080 | 0.220 | 0.003 | 0.009 |
| D | 2.800 | 3.020 | 0.110 | 0.119 |
| E | 1.500 | 1.726 | 0.059 | 0.068 |
| E1 | 2.600 | 3.000 | 0.102 | 0.118 |
| e | 0.950 (BSC) | | 0.037 (BSC) | |
| e1 | 1.800 | 2.000 | 0.071 | 0.079 |
| L | 0.300 | 0.600 | 0.012 | 0.024 |
| θ | 0° | 8° | 0° | 8° |

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