Active-PFC Constant-Voltage Controller with Primary-Side Regulation

General Description

The RT7339P is a constant voltage controller with the active Power Factor Correction (PFC). which is designed to meet the line current harmonic regulations. It drives the converter in Quasi-Resonant (QR) mode to achieve higher efficiency. By using the Primary-Side Regulation (PSR), the RT7339P controls the output voltage accurately without a shunt regulator and an opto-coupler at the secondary side, reducing the external component counts, the costs, and the volume of the driver board.

The RT7339P is compatible with the external depletion N-MOSFET to achieve fast startup and ultra-low standby power consumption.

The totem-pole gate driver with the 600mA sourcing current and 800mA sinking current provides the powerful driving capability for a power MOSFET to improve the conversion efficiency. In addition, the built-in soft drive at the turn-on transition is better for the EMI improvement.

The RT7339P integrates comprehensive protection functions for robust designs, including output over voltage protection, output short-circuit protection, output diode short-circuit protection, VDD under voltage lockout (UVLO), VDD over voltage protection (VDD OVP), over load protection, input under / over voltage protection, external / internal over temperature protection (OTP), and cycle-by-cycle current limitation.

Features

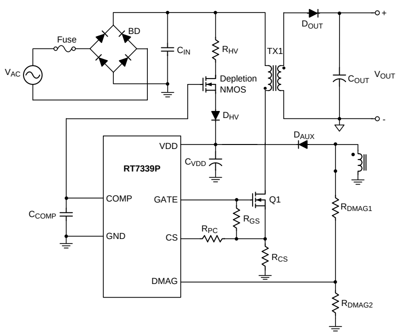
- **Tight Voltage Regulation**
- **Power Factor Correction**
- **THD Optimization (THD < 10%)**
- **Quasi-Resonant (QR) Operation**
- **Fast Startup**
- **Fast Dynamic Response**
- **Ultra-Low Standby Power Consumption**
- **Soft Drive for the Better EMI Performance**
- **Wide Supply Voltage Range (Up to 34V)**
- **Maximum Frequency Limitation (117kHz)**
- **Multiple Protection Features**
  - **Output Over Voltage Protection**
  - **Output Short-Circuit Protection**
  - **Over Load Protection**
  - **Input Under / Over Voltage Protection**
  - **Output Diode Short-Circuit Protection**
  - **VDD Over Voltage Protection**
  - **VDD Under Voltage Lockout (UVLO)**
  - **External / Internal OTP**
  - **Cycle-by-Cycle Current Limitation**

Applications

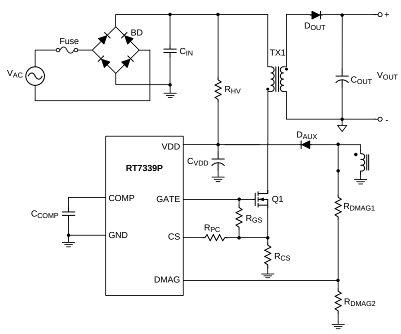
- LED Lighting
- AC-DC Adapter/Charger

Simplified Application Circuit

With Depletion N-MOS Application



Without Depletion N-MOS Application



Ordering Information

RT7339P□□

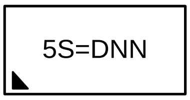
- Package Type
  E : SOT-23-6
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

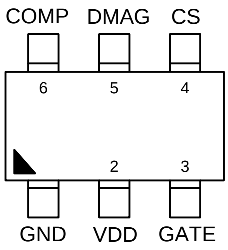
Marking Information



5S= : Product Code
DNN : Date Code

Pin Configuration

(TOP VIEW)

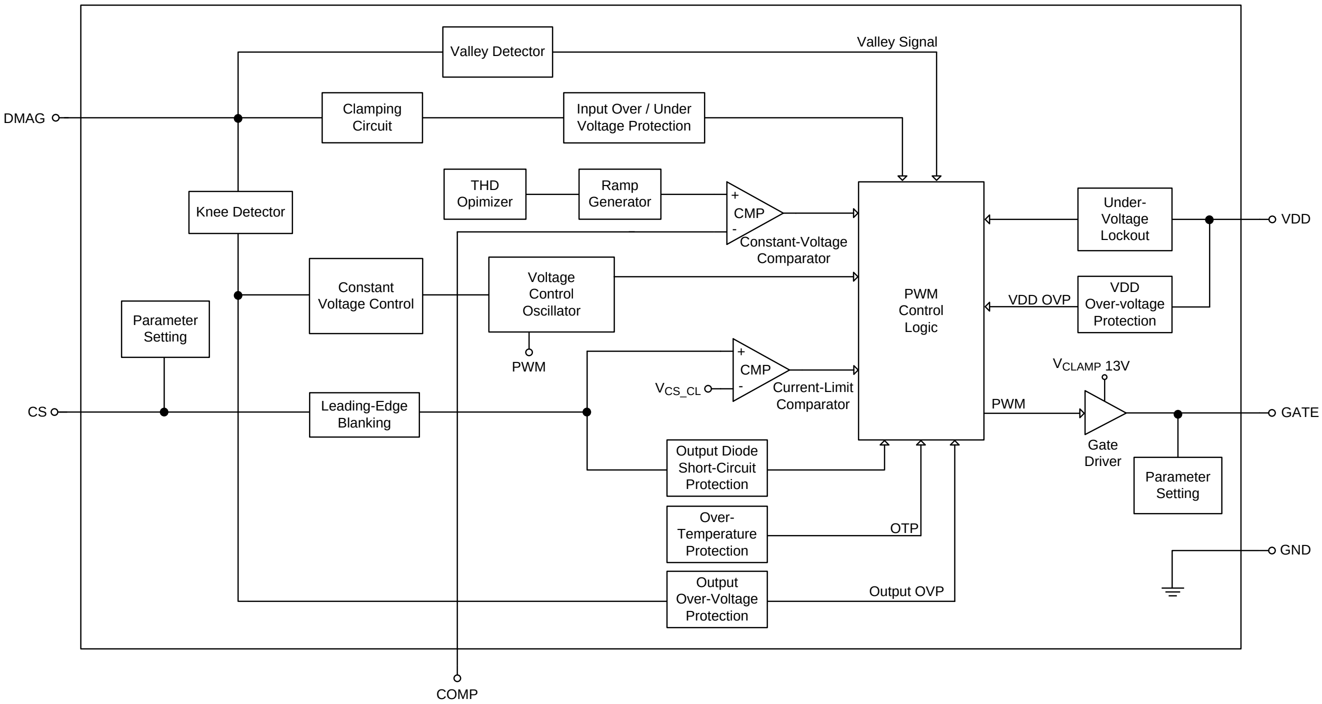


SOT-23-6

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	GND	Ground of the controller.
2	VDD	Supply voltage (V_{DD}) input. The controller will be enabled when V_{DD} exceeds V_{TH_ON} and disabled when V_{DD} is lower than V_{TH_OFF}.
3	GATE	Gate driver output for an external power MOSFET.
4	CS	Current sense input. Connect this pin to the current sense resistor.
5	DMAG	Demagnetization pin. To detect the input and the output voltage from the auxiliary winding of the transformer.
6	COMP	Compensation node. Output of the internal trans-conductance amplifier.

Functional Block Diagram



Operation

Critical-Conduction Mode (CRM) with Constant On-Time Control

Figure 1 shows a typical flyback converter with the input voltage (V_{IN}). When the main switch Q1 is turned on with a fixed on-time (t_{ON}), the peak current (I_{L_PK}) of the magnetizing inductance (L_m) can be calculated by the following equation :

$$I_{L\_PK} = \frac{V_{IN}}{L_m} \times t_{ON}$$

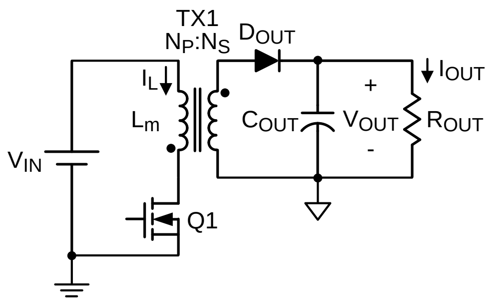


Figure 1. Typical Flyback Converter

If the input voltage is the output voltage of the full-bridge rectifier (V_{IN_PK} x $|\sin\theta|$), the inductor peak current (I_{L_PK}) can be expressed as the following equation :

$$I_{L\_PK} = \frac{V_{IN\_PK} \times |\sin(\theta)| \times t_{ON}}{L_m}$$

As shown in Figure 2, when the converter operates in CRM with the constant on-time control, the envelope of the peak inductor current is in phase with the input voltage. Thus, the high power factor can be achieved.

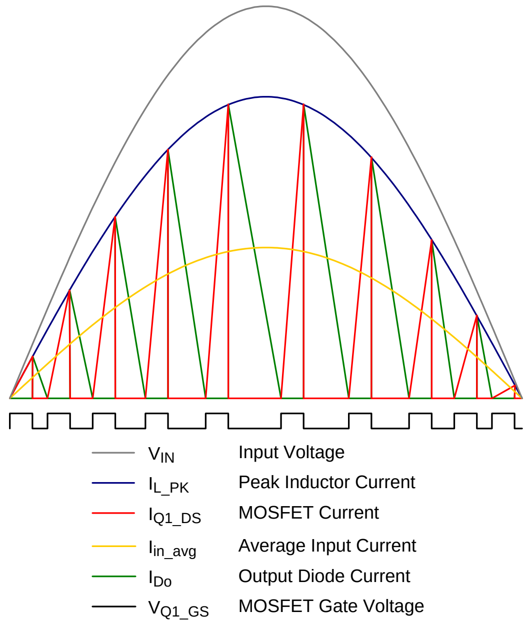


Figure 2. Inductor Current of CRM with Constant On-Time Control

The RT7339P needs no shunt regulator and opto-coupler at the secondary side to achieve the output voltage regulation. Figure 3 shows several key waveforms of a conventional flyback converter in Quasi-Resonant (QR) mode, in which V_{AUX} is the voltage on the auxiliary winding of the transformer.

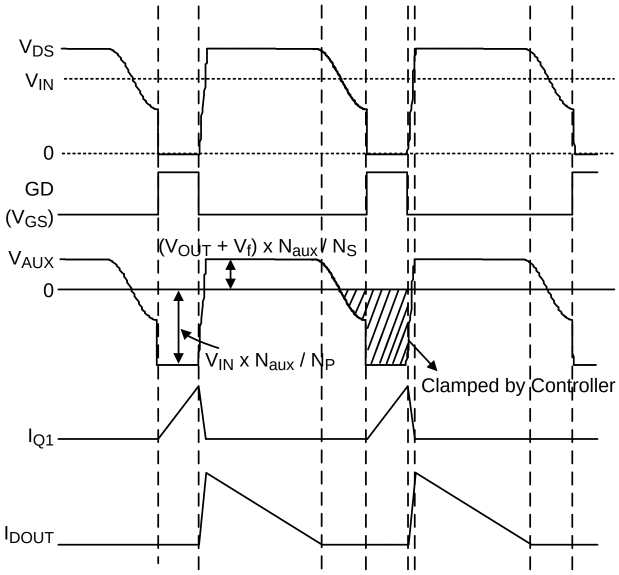


Figure 3. Key Waveforms of a Flyback Converter

Voltage Clamping Circuit

The RT7339P provides a voltage clamping circuit at DMAG pin since the voltage on the auxiliary winding is negative when the main switch is turned on. The lowest voltage on DMAG pin is clamped near zero to prevent the IC from being damaged by the negative voltage. Meanwhile, the sourcing DMAG current (I_{DMAG}), flowing through the upper resistor (R_{DMAG1}), is sampled and held to be a line-voltage-related signal for propagation delay compensation. The RT7339P embeds the programmable propagation delay compensation through CS pin. A sourcing current I_{CS} (equal to $I_{DMAG} \times K_{PC}$) applies a voltage offset ($I_{CS} \times R_{PC}$) which is proportional to line voltage on CS to compensate the propagation delay effect. Thus, the output current can be equal at high and low line voltage.

Quasi-Resonant Operation

Figure 4 illustrates how valley signal triggers PWM. If no valley signal detected for a long time, the next PWM is triggered by a starter circuit at the end of the interval (t_{START}, 127.5μs typ.). A blanking time ($t_{S(MIN)}$, 8.5μs typ.), which starts at the rising edge of the previous PWM signal, limits minimum switching period. When the $t_{S(MIN)}$ interval is on-going, all of valley signals are not allowed to trigger the next PWM signal. After the end of the $t_{S(MIN)}$ interval, the coming valley will trigger the next PWM signal. If one or more valley signals are detected during the $t_{S(MIN)}$ interval and no valley is detected after the end of the $t_{S(MIN)}$ interval, the next PWM signal will be triggered automatically at the end of the $t_{S(MIN)}$ + 5μs (typ.).

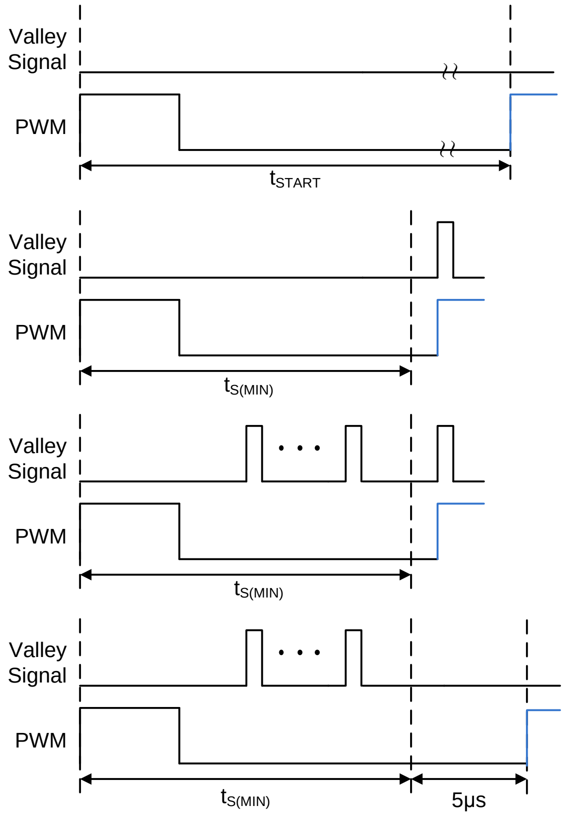


Figure 4. PWM Triggered Method

Transconductance Error Amplifier

The RT7339P implements the transconductance error amplifier with non-linear Gm design to regulate the Flyback output voltage and provide the fast dynamic response. The transconductance value is 20μA/V at normal operation. When the voltage detected by the knee detector at the DMAG pin is higher than 2.75V or lower than 2.25V, the output of the error amplifier will source or sink 20uA (typ.) maximum current at the COMP pin, respectively. As shown in Figure 5, the non-linear Gm design can provide the fast response for the dynamic load of PFC converters even though the bandwidth of the control loop is lower than the line frequency.

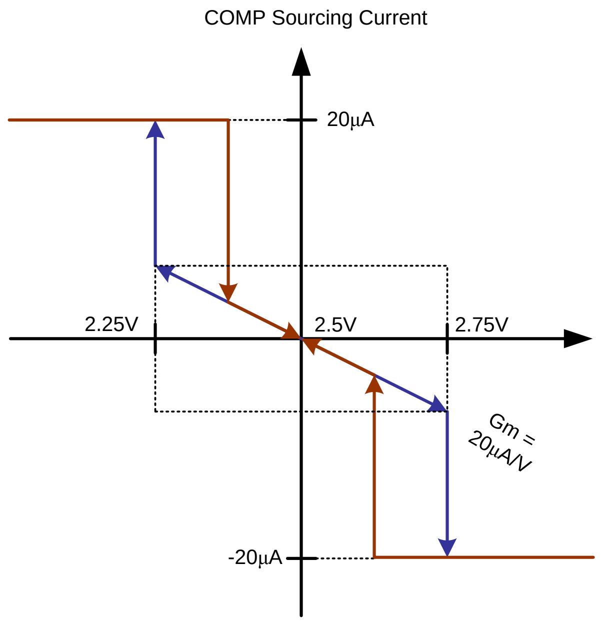


Figure 5. Non-linear Gm

Standby Mode

When COMP is lower than 0.3V for 70ms (typ.), the DMAG reference voltage (V_{DMAG_REF}, 2.5V typ.) will be reduced to the reference voltage in standby mode (V_{REF_SB}, 1.2V typ.). Therefore, the extreme low power consumption can be achieved.

Output Short-Circuit Protection

The RT7339P implements output short-circuit protection by DMAG and CS pins. Once the DMAG voltage is lower than 0.5V and the current sense voltage V_{CS} exceeds the peak current limitation (V_{CS_CL}) for few cycles, the converter will be shut down to prevent damage. It will be auto-restarted when the output is recovered.

The output short-circuit protection is masked during the first 45ms (typ.) of power on (VDD > V_{TH_ON}).

Output Diode Short-Circuit Protection

When the output diode is damaged as short-circuit, the transformer will be led to magnetic saturation and the main switch will suffer from a high current stress. To avoid the above situation, an output diode short-circuit protection is built-in. When CS voltage V_{CS} exceeds the threshold (V_{CS_SD} 0.85V typ.) of the output diode short-circuit protection, the RT7339P will shut down the PWM output (GATE pin) in few cycles to prevent the converter from damage. It will be auto-restarted when the fault condition is recovered.

VDD Under-Voltage Lockout (UVLO) and Over-Voltage Protection (VDD OVP)

The RT7339P will be enabled when VDD voltage (V_{DD}) exceeds rising UVLO threshold (V_{TH_ON}, 20V typ.) and disabled when V_{DD} is lower than falling UVLO threshold (V_{TH_OFF}, 7.3V typ.).

When V_{DD} exceeds its over-voltage threshold (V_{DD_OVP}, 37V typ.), the PWM output of the RT7339P is shut down. It will be auto-restarted when the VDD is recovered to a normal level.

Input Over-Voltage and Under-Voltage Protection

When I_{DMAG} is over the threshold current of V_{IN} over-voltage protection (I_{DMAG_OCP}) in few cycles, the GATE will shut down to avoid over stress on components. As soon as the input voltage drops below the brown-out threshold for 70ms (typ.), the controller will shut down until it recovers to the brown-in threshold.

Over Load Protection

When V_{COMP} reaches to V_{COMP_OLP} (4.8V typ.) for 178ms (typ.), the controller will shut down.

Internal and External Over-Temperature Protection (OTP)

The RT7339P provides the internal OTP function to protect the controller itself from suffering the thermal stress and permanent damage. Once the junction temperature is higher than the OTP threshold (T_{OTP_STTH}, 160°C typ.), the controller will shut down until the temperature decreases below 150°C (typ.). The external OTP function is achieved by the CS pin. If the CS voltage V_{CS}, which is during the turn-off period of the main switch, exceeds the external OTP threshold (V_{OTP_TH}) for 70ms (typ.), the controller will shut down until the fault released.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VDD ---------- –0.3V to 40V
- COMP Voltage, COMP ---------- –0.3V to 40V
- Gate Driver Output, GATE ---------- –0.3V to 18V
- Other Pins ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-6---------- 0.42W
- Package Thermal Resistance (Note 2)
  SOT-23-6, θ_{JA}---------- 235.6°C/W
  SOT-23-6, θ_{JC}---------- 32°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VDD ---------- 11V to 34V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{DD} = 30V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section (VDD)						
VDD OVP Threshold Voltage	V_{DD_OVP}		--	37	--	V
Rising UVLO Threshold Voltage	V_{TH_ON}		--	20	--	V
Falling UVLO Threshold Voltage	V_{TH_OFF}		--	7.3	--	V
VDD Holdup Mode Entry Point	V_{DD_ET}		--	8.3	--	V
VDD Holdup Mode Ending Point	V_{DD_ED}		--	9.3	--	V
External Depletion N-MOS Turn-On Threshold Voltage	$V_{DD\_AUX\_ON}$		--	4.3	--	V
Start-up Current	I_{DD_ST}	$V_{DD} = V_{TH\_ON} – 1V$	--	14.5	--	μA
Operating Current	I_{DD_OP}	V_{DD} = 15V, GATE and COMP pin open	--	900	--	μA
DMAG Section (DMAG)						
Lower Clamp Voltage	V_{DMAG_L}	I_{DMAG} = 1mA	--	100	--	mV
DMAG OVP Threshold Voltage	V_{DMAG_OVP}		--	3	--	V
Threshold Current of Brown-in Protection	I_{DMAG_BRI}		--	800	--	μA
Threshold Current of Brown-out Protection	I_{DMAG_BRO}		--	725	--	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Threshold Current of Vin Over Voltage Protection	I_{DMAG_OCP}		--	4	--	mA
High VIN Entry Level	I_{DMAG_HVSW}		--	1.75	--	mA
DMAG Reference Voltage	V_{DMAG_REF}		--	2.5	--	V
DMAG Threshold Voltage of Soft Start	V_{DMAG_SS}		--	1.2	--	V
DMAG Threshold for Output UVP	V_{TH_UVP}	$V_{TH\_UVP} = V_{DMAG\_SS}$	--	0.5	--	V
Minimum DMAG Masking Time	$t_{BK(MIN)}$	$t_{BK} = 1 + 4 \times V_{CS\text{-}PK}$, $V_{CS} = 0V$	--	1	--	μs
Maximum DMAG Masking Time	$t_{BK(MAX)}$	$t_{BK} = 1 + 4 \times V_{CS\text{-}PK}$, $V_{CS} = 0.6V$	--	3.4	--	μs
Constant Current Control Section (COMP)						
COMP Over Load Protection Threshold	V_{COMP_OLP}		--	4.8	--	V
Minimum COMP Voltage	$V_{COMP(MIN)}$		--	0.35	--	V
Standby Mode Entry Level	V_{SB_ET}	$V_{COMP} < 0.3V$	--	0.3	--	V
COMP Response Setting Threshold Voltage 1	V_{COMP_TH1}	$R_{PC} = 1.2k\Omega$	--	0.4	--	V
COMP Response Setting Threshold Voltage 2	V_{COMP_TH2}	$R_{PC} = 3k\Omega$	--	1.85	--	V
COMP Response Setting Threshold Voltage 3	V_{COMP_TH3}	$R_{PC} = 5.1k\Omega$	--	2.15	--	V
Current Sense Section (CS)						
Leading Edge Blanking Time	t_{LEB}		--	250	--	ns
Low Vin Peak Current Limit at Normal Operation	V_{CL_LV}	$I_{DMAG} < 1.71mA$	--	0.6	--	V
High Vin Peak Current Limit at Normal Operation	V_{CL_HV}	$I_{DMAG} \geq 1.75mA$	--	0.5	--	V
Peak Current Limit in VDD Holdup and Standby Mode	V_{CL_MIN}	Standby mode	--	0.1	--	V
Peak Current Shutdown Voltage Threshold	V_{CS_SD}		--	0.85	--	V
Threshold Voltage for External OTP	V_{OTP_TH}	$V_{DMAG} = 2.5V$, $V_{CS} = 4/15 * V_{DMAG}$	--	0.67	--	V
Gate Driving Section (GATE)						
Rising Time	t_R	$V_{DD} = 15V$, $C_L = 1nF$ (10% to 90%)	--	270	--	ns
Falling Time	t_F	$V_{DD} = 15V$, $C_L = 1nF$ (10% to 90%)	--	40	--	ns
Gate Output Clamping Voltage	V_{CLAMP}	$V_{DD} = 15V$	--	13	--	V
Internal Pull Low Resistor	R_{GATE}	$VDD < V_{TH\_ON}$, before startup	--	40	--	kΩ
Timing Control Section						
Minimum Switching Period	$t_{S(MIN)}$	$V_{COMP} > 2V$	--	8.5	--	μs
Minimum Switching Period in Green Mode	$t_{S(MIN)\_GM}$	$V_{COMP} < 0.5V$	--	2	--	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Start Time During Startup and Normal Operation	t_{START}	V_{COMP} > 2V	--	31.9	--	μs
Max. Start time in Green Mode	t_{START_GM}	V_{COMP} < 0.5V	--	7.5	--	ms
Minimum On Time	$t_{ON(MIN)\_LV}$		--	800	--	ns
	$t_{ON(MIN)\_HV}$		--	600	--	ns
Maximum On Time	$t_{ON(MAX)}$		--	20	--	μs
Over-Temperature Protection (OTP) Section						
Initial Over Temperature Protection Threshold	T_{OTP_INTH}		--	150	--	°C
Over Temperature Protection Threshold After Start-up	T_{OTP_STTH}		--	160	--	°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a low effective-thermal-conductivity two-layer test board on a JEDEC thermal measurement standard.

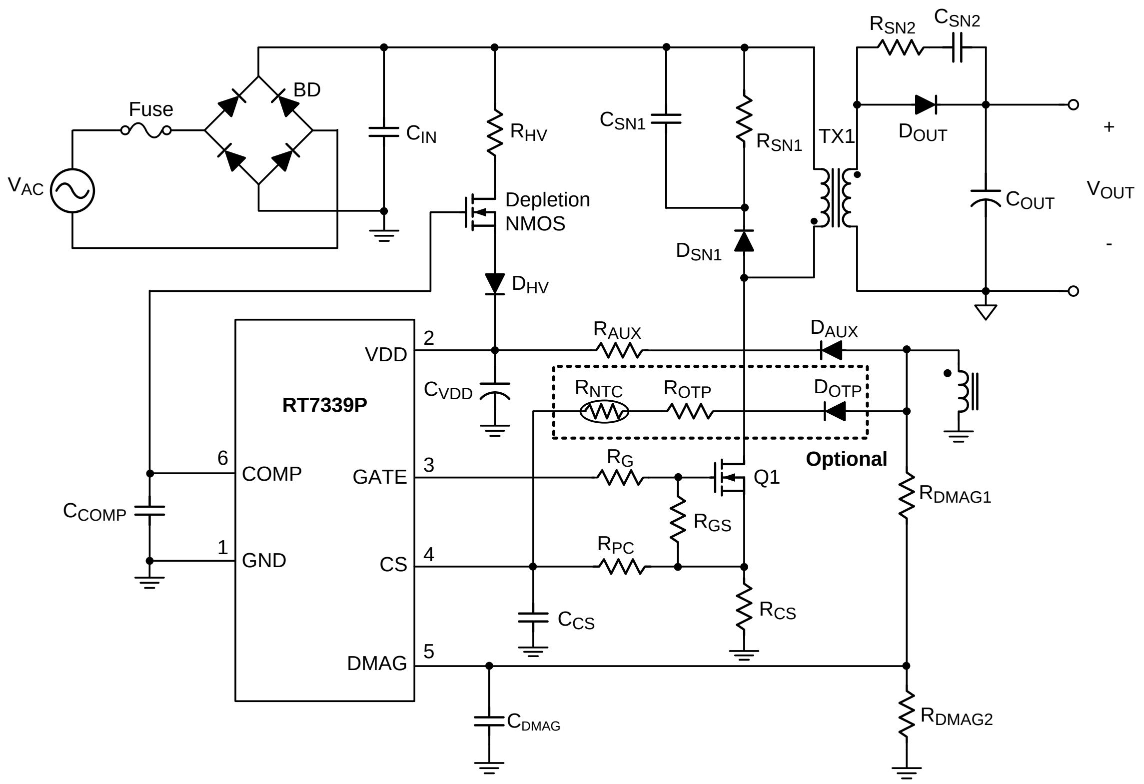
Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

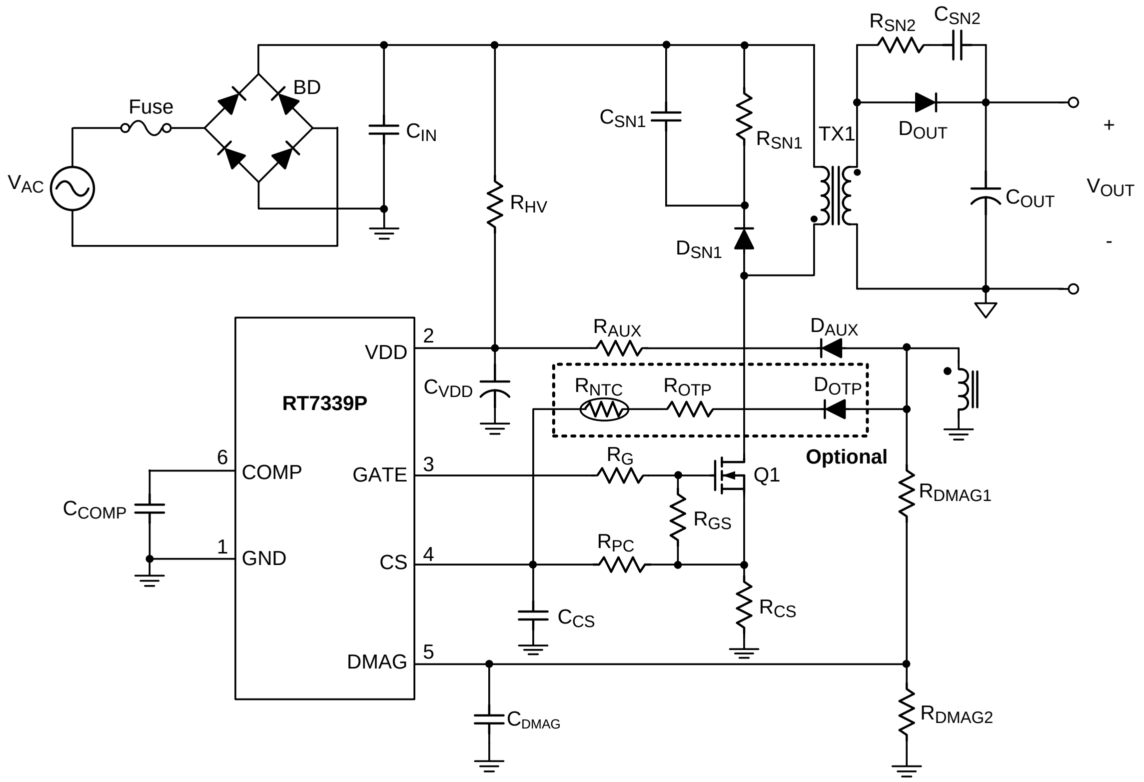
Note 5. Guarantee by design.

Typical Application Circuit

PSR Flyback Application Circuit with Depletion N-MOS



PSR Flyback Application Circuit without Depletion N-MOS



Application Information

COMP Voltage Design

The COMP voltage, V_{COMP}, can be expressed as follows :

$$V_{COMP} = \frac{V_{THDO} \times G_{m\_ramp} \times t_{on\_pk}^2 \times f_{s\_pk}}{C_{ramp}} + V_D$$

where t_{on_pk} and f_{s_pk} are the peak values at V_{IN_pk}, G_{m_ramp} and C_{ramp} are the fixed parameters in RT7339P and the typical values are : G_{m_ramp} = 2.7μA/V, C_{ramp} = 6.5pF. V_D is the offset of the constant-voltage comparator and its typical value is 2V.

V_{THDO} is the input voltage of the THD optimizer and it can be selected as different voltages by the external Gate-to-Source resistor R_{GS}. The recommended R_{GS} is 22kΩ or 47kΩ, and the corresponding values of V_{THDO} are 1.2V and 0.9V, respectively. It is recommended to design V_{COMP} = 3.5 to 4.2V. If V_{COMP} is over 4.2V, the output voltage regulation may be affected.

Input Under-Voltage Protection Setting

The input voltage is detected by R_{DMAG1}, which is used to set the input UV level (V_{IN_UVP}). Thus, R_{DMAG1} can be determined by the following equation :

$$R_{DMAG1} = V_{IN\_pk} \times \frac{N_A}{N_P} \times \frac{1}{I_{DMAG\_BRI}}$$

where I_{DMAG_BRI} is the fixed parameters in RT7339P and its typical value is 800μA.

Output Voltage Setting

The output voltage is sensed and regulated by the DMAG pin. When the switch is turned off, the reflected output voltage at the auxiliary winding can be obtained and expressed as follows :

$$V_{REF} = (V_{OUT} + V_F) \times \frac{N_A}{N_S} \times \frac{R_{DMAG2}}{R_{DMAG1} + R_{DMAG2}}$$

where V_F is the forward voltage of the output diode. V_{REF} is the reference voltage of RT7339P and its typical value is 2.5V.

COMP Response Setting

The RT7339P features the adjustable response to improve the stability at light load. The threshold voltage is set by the resistor R_{PC} and the corresponding value can be found in the following table :

R_{PC}	1.2kΩ	3kΩ	5.1kΩ
V_{COMP_TH}	0.4V	1.85V	2.15V

where V_{COMP_TH} is the COMP response setting threshold. When V_{COMP} is lower than V_{COMP_TH}, the RT7339P is switched to fast response.

Current Limit Setting

Cycle by cycle current limit is achieved by sensing the voltage on the current sense resistor R_{CS}. It is recommended that the maximum peak voltage of the CS pin is designed at 80% of the current limit level. Thus, RCS can be determined by the equation as :

$$R_{CS} = \frac{V_{CL\_LV}}{I_{P\_pk}} \times 80\%$$

where I_{P_pk} is the maximum peak inductor current at the primary side.

Adaptive Blanking Time

When the MOSFET is turned off, the leakage inductance of the transformer and parasitic capacitance (C_{OSS}) of the MOSFET induce resonance waveform on the DMAG pin. The resonance waveform may make the controller false trigger the DMAG OVP, and it may cause the controller operate in unstable condition. As load increases, the resonance time also increases. It is recommended to add a 10pF to 47pF bypass capacitor, and it should be as close to DMAG pin as possible. The larger bypass capacitor may cause phase shift on DMAG waveform. Therefore, the output voltage regulation will be affected.

To avoid the above issue, the RT7339P provides adaptive blanking time (t_{BK}). It varies with the peak voltage of the CS pin (V_{CS_PK}), as shown by the following formula :

t_{BK} = 1μs + V_{CS_PK} x 4μs/V (typ.)

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a SOT-23-6 package, the thermal resistance, θ_{JA}, is 235.6°C/W on a standard JEDEC low effective-thermal-conductivity two-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / (235.6°C/W) = 0.42W for a SOT-23-6 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

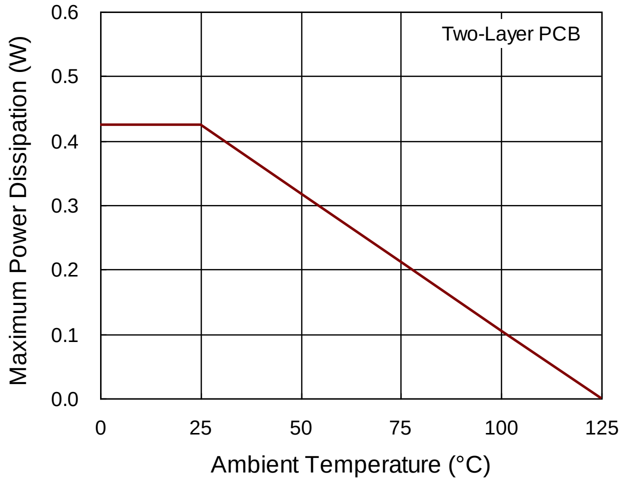


Figure 6. Derating Curve of Maximum Power Dissipation

Layout Considerations

A proper PCB layout can abate unknown noise interference and EMI issue in the switching power supply. Please refer to the guidelines when designing a PCB layout for switching power supply :

- The current path(1) from the input capacitor, transformer, MOSFET, R_{CS} returning to input capacitor is a high frequency current loop. The path(2) from GATE pin, MOSFET, R_{CS} returning to the ground of the IC is also a high frequency current loop. They must be as short as possible to decrease noise coupling and kept a space to other low voltage traces, such as IC control circuit paths, especially. Besides, the path between MOSFET ground(b) and IC ground(d) is recommended to be as short as possible, too.
- The path(3) from RCD snubber circuit to MOSFET is a high switching loop. Keep it as small as possible.
- The path(4) from the input capacitor to VDD pin is a high voltage loop. Keep a space from path(4) to other low voltage traces.
- It is good for reducing noise, output ripple and EMI issue to separate ground traces of the input capacitor(a), MOSFET(b), auxiliary winding(c) and IC control circuit(d). Finally, connect them together at the input capacitor ground(a). The areas of these ground traces should be kept large.
-

- To reduce the parasitic trace inductance and EMI, the area of the loop connecting to the secondary winding, the output diode, and the output filter capacitor must be minimized. In addition, the sufficient copper area at the anode and cathode terminal of the output diode can help for heat-sinking. It is recommended to apply the larger area at the quiescent cathode terminal. The large anode area will induce high-frequency radiated EMI.

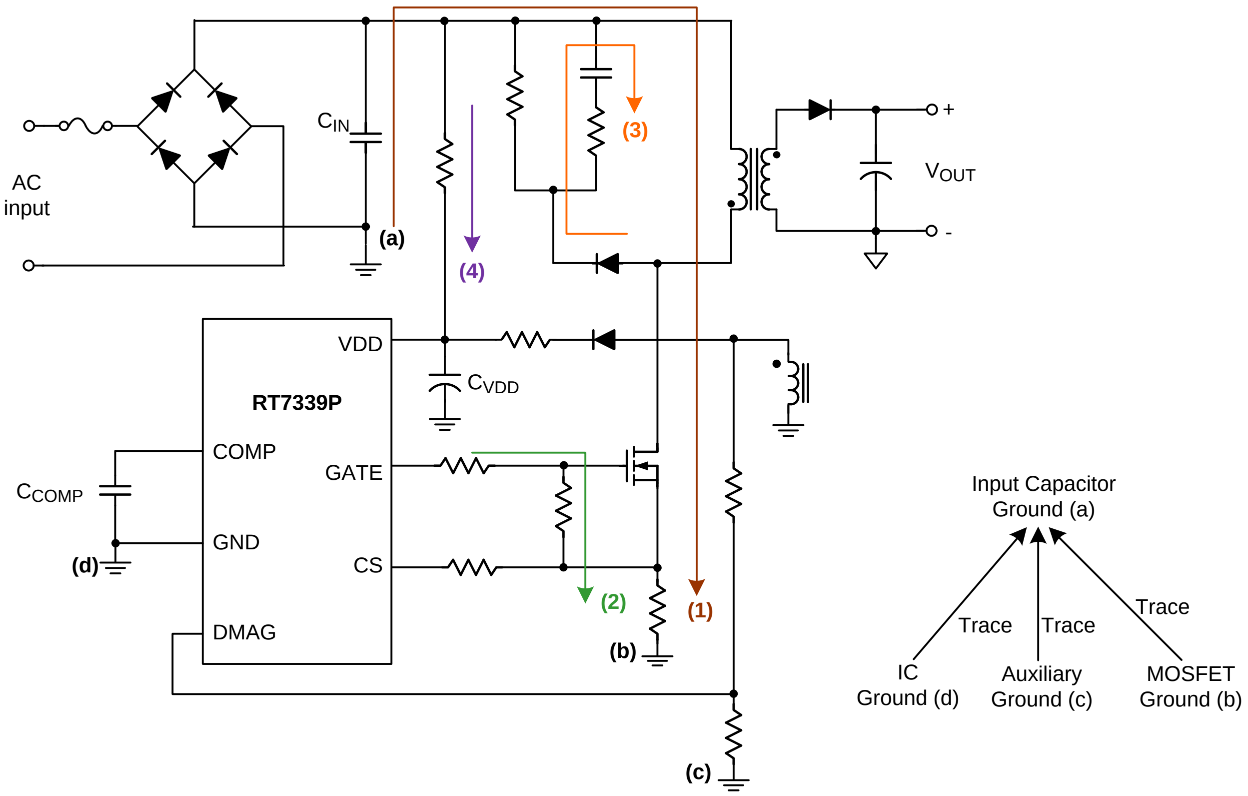
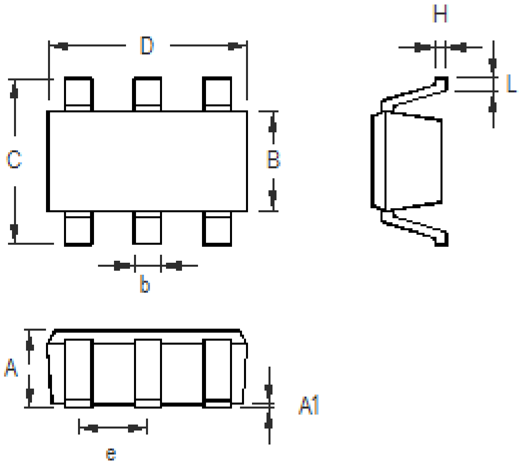


Figure 7. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package

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Datasheet Revision History

Version	Date	Item	Description
P00	2018/8/22		First Edition