

Final

16Gb E-die NAND Flash

Multi-Level-Cell (2bit/cell)

datasheet

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Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>	<u>Editor</u>
0.0	1. Initial issue	Jun. 12, 2009	Advance	
0.1	1. Pin configuration is changed. 2. tREA is changed from 20ns to 25ns. 3. Memory cell array is amended. 4. Row address is modified. 5. Dummy busy time for Two-Plane Program(tDBSY) is deleted.	Oct. 21, 2009	Advance	
0.2	1. Pin configuration is changed.	Oct. 21, 2009	Advance	
0.3	1. tRC/tWC is changed from 30ns to 20ns. 2. The Parameter related tRC/tWC is changed	Nov. 6, 2009	Advance	
0.4	1. 52LGA (11x14) QDP is added	Nov. 13, 2009	Advance	S.M.Lee
0.5	1. AC character's changed.	Jan. 20, 2010	Advance	S.M.Lee
0.9	1. Part ID K9LBG08U0E and K9HCG08U1E are added.	Mar. 09, 2010	Final	S.M.Lee
0.9.1	1. tR 300->400 changed. 2. K9HCG08U5E is deleted. 3.Package Dimensions of 48-TSOP are amended.	Mar. 31, 2010	Final	S.M.Lee

芯博源电子 QQ793013654

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1.0 INTRODUCTION

1.1 Product List

Part Number	Density	Interface	Vcc Range	Organization	PKG Type
K9GAG08U0E-S	16Gb	Conventional	2.7V ~ 3.6V	x8	48TSOP1
K9LBG08U0E-S	32Gb				
K9HCG08U1E-S	64Gb				

1.2 Features

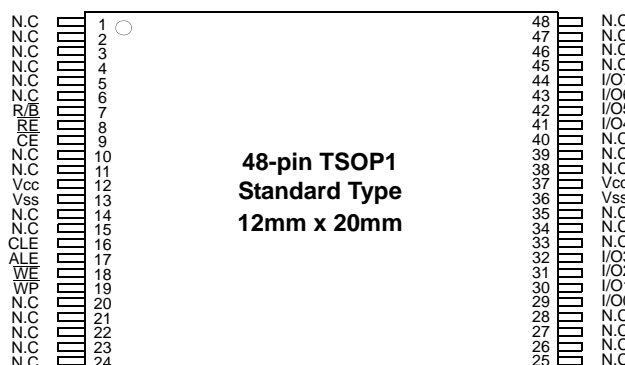
- Voltage Supply
 - 3.3V Device : 2.7V ~ 3.6V
- Organization
 - Memory Cell Array : (2,076M x 110.49K) x 8bit
 - Data Register : (8K + 436) x 8bit
- Automatic Program and Erase
 - Page Program : (8K + 436)Byte
 - Block Erase : (1M + 54.5K)Byte
- Page Read Operation
 - Page Size : (8K + 436)Byte
 - Random Read : 400 μ s(Max.)
 - Serial Access : 30ns(Min.)
- Memory Cell : 2bit / Memory Cell
- Fast Write Cycle Time
 - Program time : 1.2ms(Typ.)
 - Block Erase Time : 1.5ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
 - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
 - ECC Requirement : 24bit/(1K +54.5)Byte
 - Endurance & Data Retention : Please refer to the qualification report
- Command Register Operation
- Unique ID for Copyright Protection
- Package :
 - K9GAG08U0E-SCB0/SIB0 : Pb-Halogen FREE PACKAGE
48 - Pin TSOP1 (12 x 20 / 0.5 mm pitch)
 - K9LBG08U0E-SCB0/SIB0 : Pb-Halogen FREE PACKAGE
48 - Pin TSOP1 (12 x 20 / 0.5 mm pitch)
 - K9HCG08U1E-SCB0/SIB0 : Pb-Halogen FREE PACKAGE
48 - Pin TSOP1 (12 x 20 / 0.5 mm pitch)

1.3 General Description

The device is offered in 3.3V Vcc. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation can be performed in typical 1.2ms on the 8,628-byte page and an erase operation can be performed in typical 1.5ms on a (1M+54.5K)byte block. Data in the data register can be read out at 30ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9GAG08U0E's extended reliability of P/E cycles which are presented in the Qualification report by providing ECC(Error Correcting Code) with real time mapping-out algorithm. The K9GAG08U0E is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

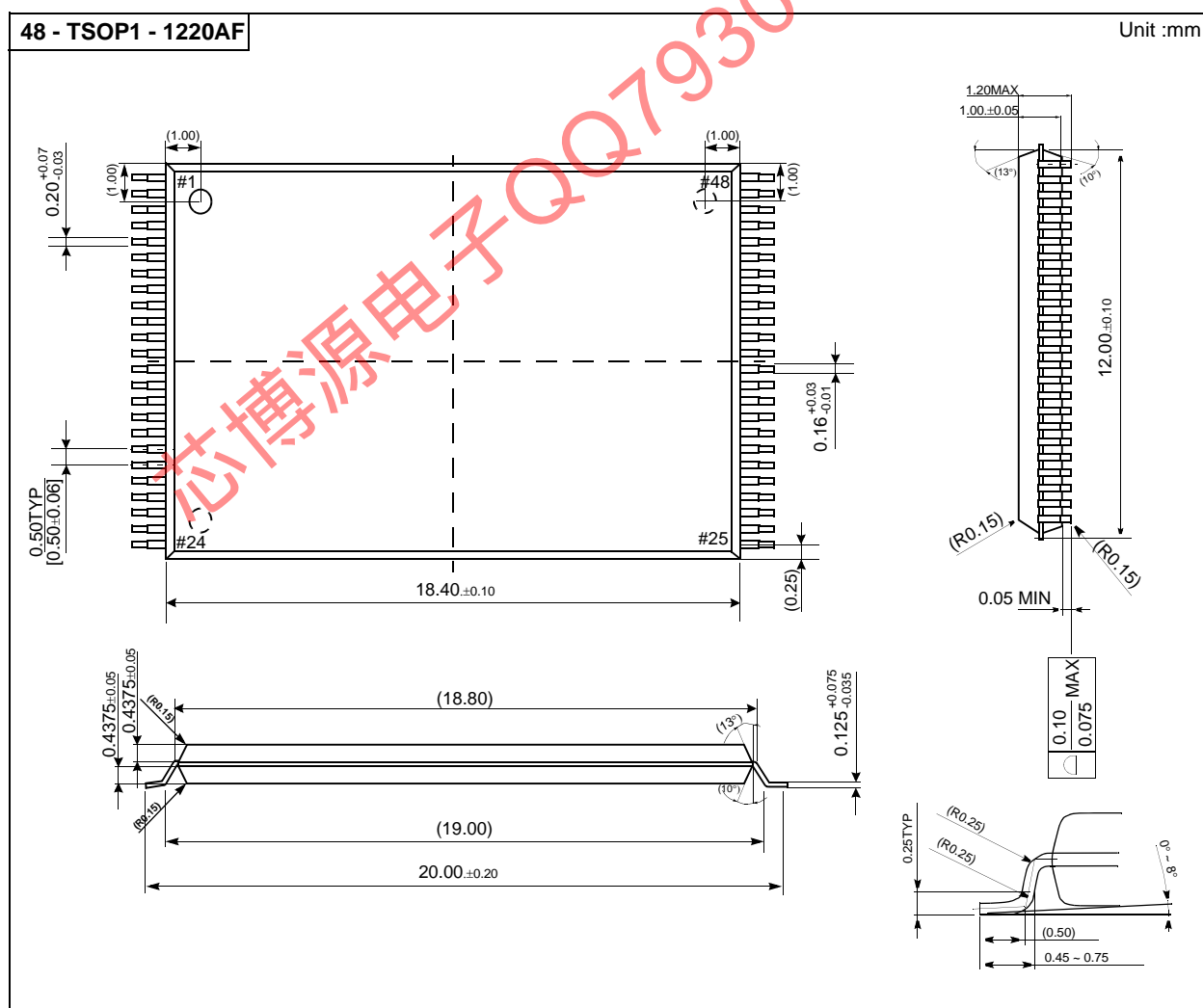
1.4 Pin Configuration (48TSOP)

K9GAG08U0E-SCB0/SIB0
K9LBG08U0E-SCB0/SIB0



1.4.1 Package Dimensions

48-PIN LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)



1.6 Pin Description

Pin Name	Pin Function
I/O ₀ ~ I/O ₇	DATA INPUTS/OUTPUTS The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	COMMAND LATCH ENABLE The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WE signal.
ALE	ADDRESS LATCH ENABLE The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WE with ALE high.
$\overline{\text{CE}}$	CHIP ENABLE The $\overline{\text{CE}}$ input is the device selection control. When the device is in the Busy state, $\overline{\text{CE}}$ high is ignored, and the device does not return to standby mode in program or erase operation.
$\overline{\text{RE}}$	READ ENABLE The RE input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{\text{RE}}$ which also increments the internal column address counter by one.
$\overline{\text{WE}}$	WRITE ENABLE The WE input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{\text{WE}}$ pulse.
$\overline{\text{WP}}$	WRITE PROTECT The WP pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{\text{WP}}$ pin is active low.
R/B	READY/BUSY OUTPUT The R/B output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
Vcc	POWER Vcc is the power supply for device.
Vss	GROUND
N.C	NO CONNECTION Lead is not internally connected.

NOTE :
Connect all VCC and VSS pins of each device to common power supply outputs.
Do not leave VCC or VSS disconnected.

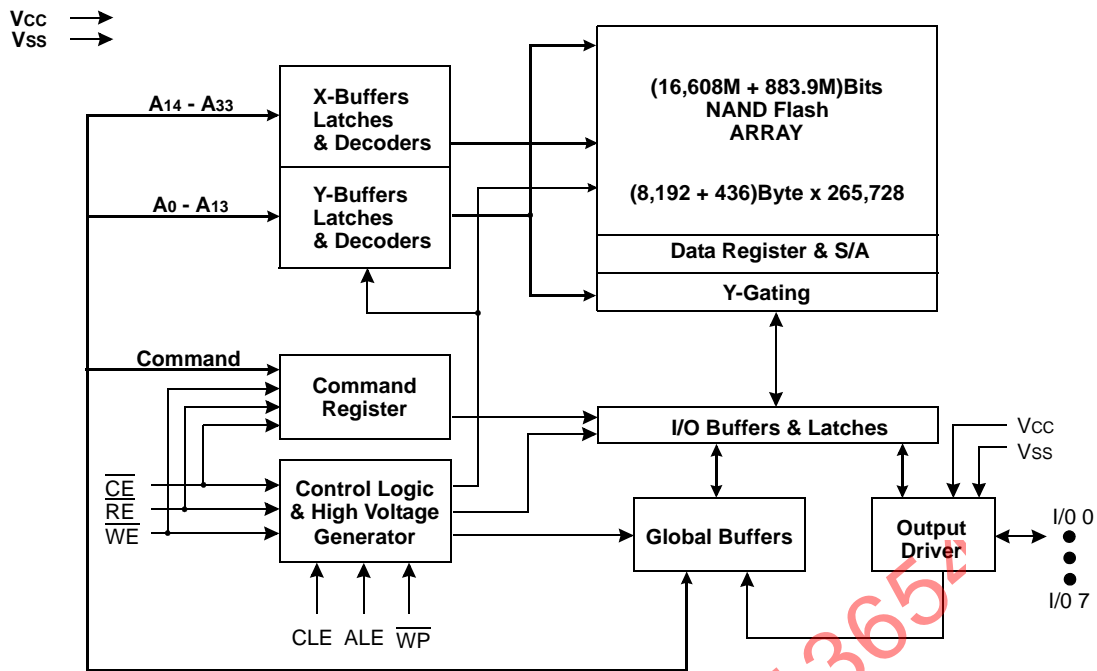


Figure 1. K9GAG08U0E Functional Block Diagram

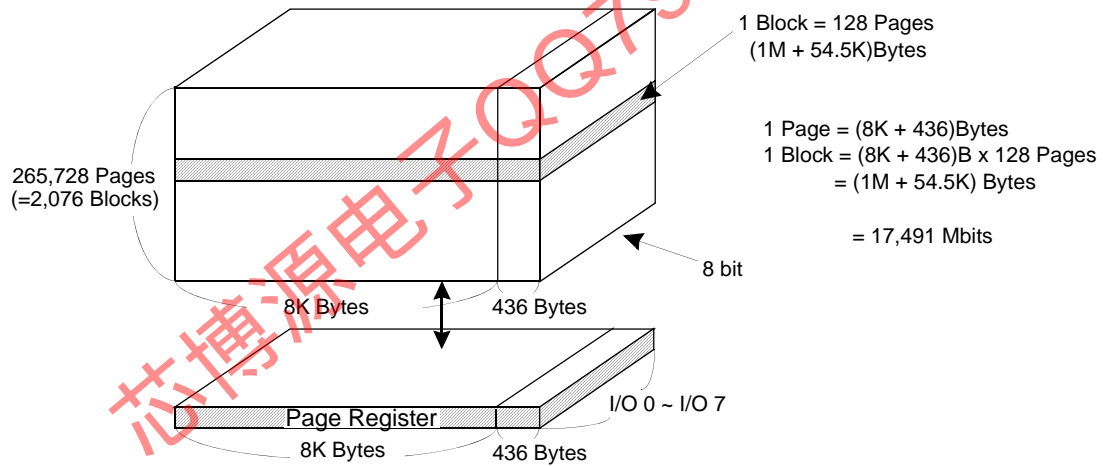


Figure 2. K9GAG08U0E Array Organization

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	A12	A13	*L	*L
3rd Cycle	A14	A15	A16	A17	A18	A19	A20	A21
4th Cycle	A22	A23	A24	A25	A26	A27	A28	A29
5th Cycle	A30	A31	A32	A33*	*L	*L	*L	*L

Column Address

Row Address;

Page Address : A14 ~ A20

Block Address : A21 ~ A32

*A33 : Chip address for
K9LBG08U0E, K9HCG08U1E

NOTE :

Column Address : Starting Address of the Register.

* L must be set to 'Low'.

* The device ignores any additional input of address cycles than required.

* Row Address consists of Page address (A14 ~ A20) & Block address(A21 ~ the last Address)

2.0 PRODUCT INTRODUCTION

NAND Flash Memory has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing \overline{WE} to low while \overline{CE} is low. Those are latched on the rising edge of \overline{WE} . Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc. require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution.- Page Read and Page Program need the same five address cycles following the required command input. In Block Erase operation, however, only the three row address cycles are used. Device operations are selected by writing specific commands into the command register. The table below defines the specific commands.

[Table 1] Command Sets

Function	1st Set	2nd Set	Acceptable Command during Busy
Read	00h	30h	
Read for Copy Back	00h	35h	
Cache Read	31h	-	
Read Start for Last Page Cache Read	3Fh	-	
Page Program	80h	10h	
Cache Program	80h	15h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input ⁽¹⁾	85h	-	
Random Data Output ⁽¹⁾	05h	E0h	
Read ID	90h	-	
Read Status	70h	-	O
Chip Status1	F1h	-	O
Chip Status2	F2h	-	O
Reset	FFh	-	O

NOTE :

1) Random Data Input/Output can be executed in a page.

CAUTION : Any undefined command inputs are prohibited except for above command set of Table 1.

2.1 Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to Vss		VCC	-0.6 to + 4.6	V
		VIN	-0.6 to + 4.6	
		VIO	-0.6 to VCC+0.3 (<4.6V)	
Storage Temperature	K9XXG08UXE-XCB0	TSTG	-65 to +100	°C
	K9XXG08UXE-XIB0			
Short Circuit Current		Ios	5	mA

NOTE :

- 1) Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
Maximum DC voltage on input/output pins is VCC+0.3V which, during transitions, may overshoot to VCC+2.0V for periods <20ns.
- 2) Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2.2 Recommended Operating Conditions

(Voltage reference to GND, K9XXG08XXE-XCB0 :TA=0 to 70°C⁽¹⁾, K9XXG08XXE-XIB0:TA=-40 to 85°C⁽¹⁾)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	VCC	2.7	3.3	3.6	V
Supply Voltage	VSS	0	0	0	V

NOTE:

- 1) Data retention is not guaranteed on Operating condition temperature over/under.

2.3 Dc And Operating Characteristics(Recommended Operating Conditions Otherwise Noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Current	Page Read with Serial Access	Icc1 ⁽⁴⁾	tRC=30ns CE=VIL, IOUT=0mA	-	30	50	mA
	Program	Icc2 ⁽⁴⁾	-				
	Erase	Icc3 ⁽⁴⁾	-				
Stand-by Current(CMOS)		ISB ⁽³⁾	CE=VCC-0.2, WP=0V/VCC	-	10	50	μA
Input Leakage Current		II ⁽⁵⁾	VIN=0 to VCC(max)	-	-	±10	
Output Leakage Current		ILO ⁽⁵⁾	VOU=0 to VCC(max)	-	-	±10	
Input High Voltage		VIH ⁽¹⁾	-	0.8 xVCC	-	VCC +0.3	V
Input Low Voltage, All inputs		VIL ⁽¹⁾	-	-0.3	-	0.2 xVCC	
Output High Voltage Level		VOH	K9GAG08U0E :IOH=-400μA	2.4	-	-	
Output Low Voltage Level		VOL	K9GAG08U0E :IOL=2.1mA	-	-	0.4	
Output Low Current(R/B)		IOL(R/B)	K9GAG08U0E :VOL=0.4V	8	10	-	mA

NOTE :

- 1) VIL can undershoot to -0.4V and VIH can overshoot to VCC +0.4V for durations of 20 ns or less.
- 2) Typical value is measured at VCC=3.3V, TA=25°C. Not 100% tested.
- 3) The Typical value of the K9LBG08U0E's ISB is 20μA and the maximum value is 100μA
The Typical value of the K9HCG08U1E's ISB is 40μA and the maximum value is 200μA
- 4) The Typical value of K9LBG08U0E, K9HCG08U1E's Icc1, Icc2 and Icc3 are 35mA and the maximum values are 55mA.
- 5) The maximum value of K9LBG08U0E's is ±20μA.
The maximum value of K9HCG08U1E's is ±40μA.

2.4 Valid Block

Parameter	Symbol	Min	Typ.	Max	Unit
K9GAG08U0E	NVB	2,018	-	2,076	Blocks
K9LBG08U0E		4,036		4,152	
K9HCG08U1E		8,072		8,304	

NOTE :

- 1) The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of invalid blocks.
- 2) The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment

2.5 Ac Test Condition

(K9XXG08XXE-XCB0 :TA=0 to 70°C, K9XXG08XXE-XIB0:TA=-40 to 85°C, K9XXG08UXE: Vcc=2.7V ~ 3.3V, unless otherwise noted)

Parameter	K9XXG08UXE
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc/2
Output Load	1 TTL GATE and CL=50pF

2.6 Capacitance(Ta=25°C, Vcc=3.3v, F=1.0mhz)

Item	Symbol	Test Condition	K9GAG08U0E		K9LBG08U0E		K9HCG08U1E		Unit
			Min	Max	Min	Max	Min	Max	
Input/Output Capacitance	C _{I/O}	V _{IL} =0V	-	8	-	13	-	23	pF
	C _{I/O(W)*}		-	5	-	10	-	20	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	8	-	13	-	23	pF
	C _{IN(W)*}		-	5	-	10	-	20	pF

NOTE :

- 1) Capacitance is periodically sampled and not 100% tested.
- 2) C_{I/O(W)} and C_{IN(W)} are tested at wafer level.

2.7 Mode Selection

CLE	ALE	CE	WE	RE	WP	Mode	
H	L	L		H	X	Read Mode	Command Input
L	H	L		H	X		Address Input(5clock)
H	L	L		H	H	Write Mode	Command Input
L	H	L		H	H		Address Input(5clock)
L	L	L		H	H	Data Input	
L	L	L	H		X	Data Output	
X	X	X	X	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X ⁽¹⁾	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc ⁽²⁾	Stand-by	

NOTE :

- 1) X can be V_{IL} or V_{IH}.
- 2) WP should be biased to CMOS high or CMOS low for standby.

2.8 Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	tPROG	-	1.2	5	ms
Dummy Busy Time for Cache Program	tcBSY ⁽⁴⁾	-	-	5	ms
Number of Partial Program Cycles in the Same Page	Nop	-	-	1	cycle
Block Erase Time	tBERS	-	1.5	10	ms

NOTE:

- 1) Typical program time is measured at Vcc=3.3V, TA=25°C. Not 100% tested.
- 2) Typical Program time is defined as the time within which more than 50% of the whole pages are programmed at 3.3V Vcc and 25°C temperature.
- 3) Within a same block, program time(tPROG) of page group A is faster than that of page group B. Typical tPROG is the average program time of the page group A and B(Table 5).
Page Group A: Page 0, 1, 3, 5, 7, ... , 77,79,7B,7D
Page Group B: Page 2, 4, 6, 8, 0A, ... , 7A,7C,7E,7F
- 4) tcBSY depends on the timing between internal programming time and data in time.

2.9 AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	tCLS ⁽¹⁾	15	-	ns
CLE Hold Time	tCLH	5	-	ns
$\overline{\text{CE}}$ Setup Time	tCS ⁽¹⁾	25	-	ns
$\overline{\text{CE}}$ Hold Time	tCH	5	-	ns
$\overline{\text{WE}}$ Pulse Width	tWP	15	-	ns
ALE Setup Time	tALS ⁽¹⁾	15	-	ns
ALE Hold Time	tALH	5	-	ns
Data Setup Time	tDS ⁽¹⁾	15	-	ns
Data Hold Time	tDH	5	-	ns
Write Cycle Time	tWC	30	-	ns
$\overline{\text{WE}}$ High Hold Time	tWH	10	-	ns
Address to Data Loading Time	tADL ⁽²⁾	300	-	ns

- NOTES :**
1. The transition of the corresponding control pins must occur only once while $\overline{\text{WE}}$ is held low
 2. tADL is the time from the $\overline{\text{WE}}$ rising edge of final address cycle to the $\overline{\text{WE}}$ rising edge of first data cycle

2.10 AC Characteristics for Operation

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	tR	-	400	μs
ALE to \overline{RE} Delay	tAR	10	-	ns
CLE to \overline{RE} Delay	tCLR	10	-	ns
Ready to \overline{RE} Low	tRR	20	-	ns
\overline{RE} Pulse Width	tRP	15	-	ns
\overline{WE} High to Busy	tWB	-	100	ns
WP High to \overline{WE} Low	tWW	100	-	ns
Read Cycle Time	tRC	30	-	ns
\overline{RE} Access Time	tREA	-	25	ns
\overline{CE} Access Time	tCEA	-	35	ns
\overline{RE} High to Output Hi-Z	tRHZ	-	100	ns
\overline{CE} High to Output Hi-Z	tCHZ	-	30	ns
\overline{CE} High to ALE or CLE Don't Care	tCSD	0	-	ns
\overline{RE} High to Output Hold	tRHOH	15	-	ns
\overline{RE} Low to Output Hold	tRLOH	5	-	ns
\overline{RE} High Hold Time	tREH	10	-	ns
Output Hi-Z to \overline{RE} Low	tIR	0	-	ns
\overline{RE} High to \overline{WE} Low	tRHW	100	-	ns
\overline{WE} High to \overline{RE} Low	tWHR	60	-	ns
Device Resetting Time(Read/Program/Erase)	tRST	-	10/30/500 ⁽¹⁾	μs
Cache Busy in Read Cache (following 31h and 3Fh)	tDCBSYR	-	400	μs

Note :

1) If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 10us.

3.0 NAND FLASH TECHNICAL NOTES

3.1 Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Samsung. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.

3.2 Initial Invalid Block(s)

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. Samsung makes sure that the first or the last page of every initial invalid block has non-FFh data at the column address of 0 or 8,192. The initial invalid block information is also erasable in most cases, and it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the initial invalid block information and create the initial invalid block table via the following suggested flow chart. Any intentional erasure of the initial invalid block information is prohibited

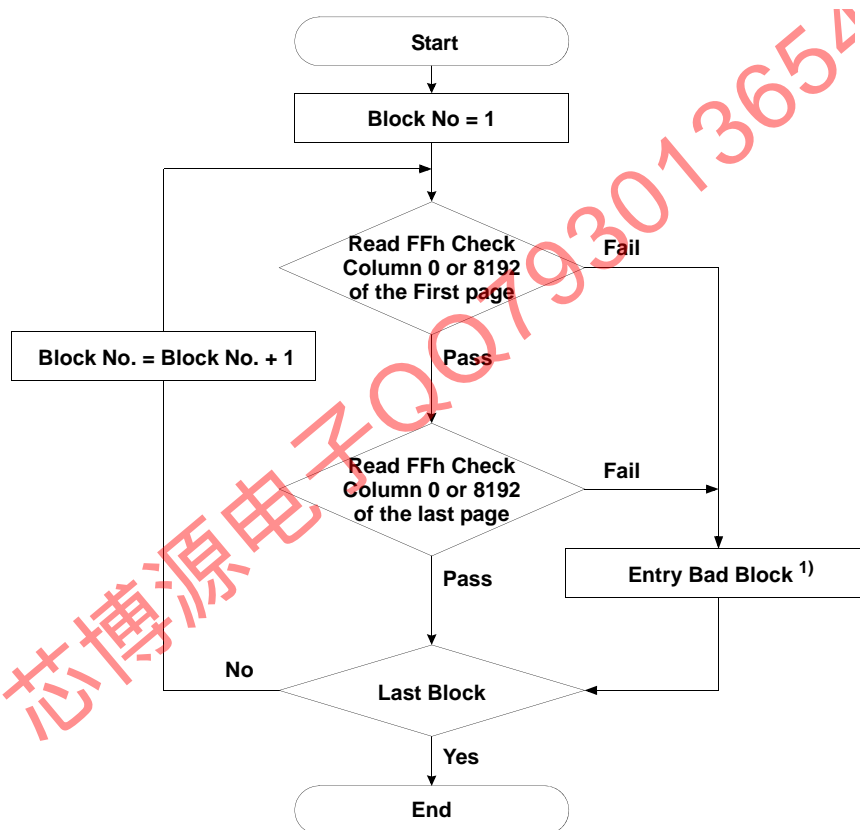


Figure 3. Flow Chart to Create Initial Invalid Block Table

NOTE :

1) No Erase Operation is allowed to detected bad block

3.3 Error in write or read operation

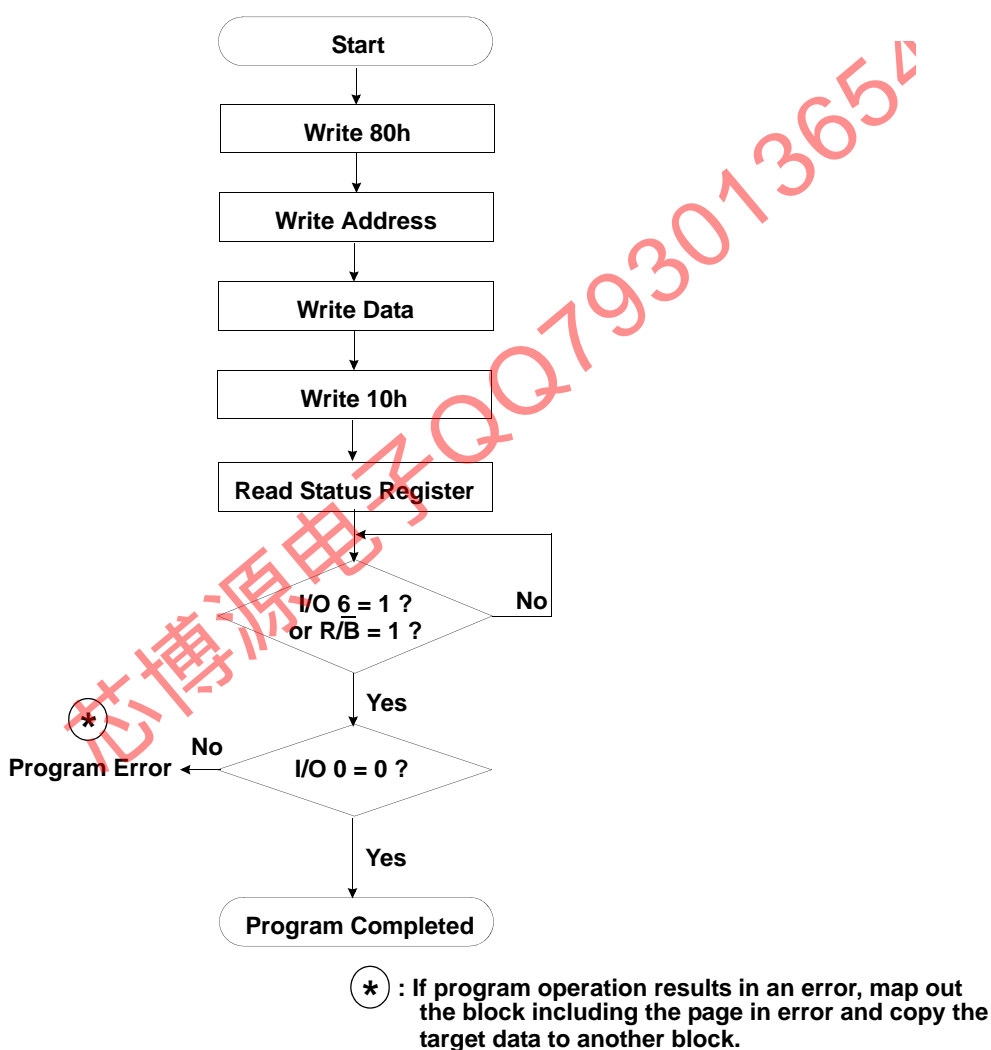
Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. Block replacement should be done upon erase or program error.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement
Read	Up to 24 Bit Failure	Verify ECC -> ECC Correction

ECC

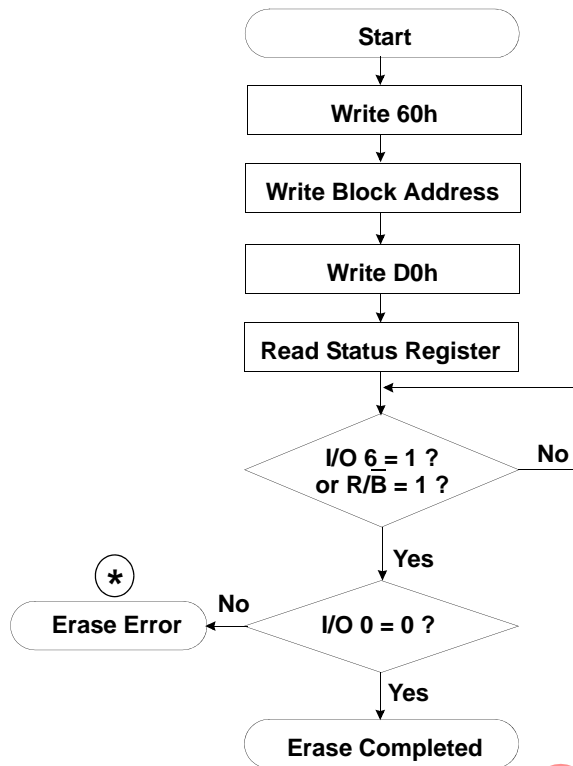
: Error Correcting Code --> RS Code or BCH Code etc.
Example) 24bit correction / 1K+54.5 byte

Program Flow Chart



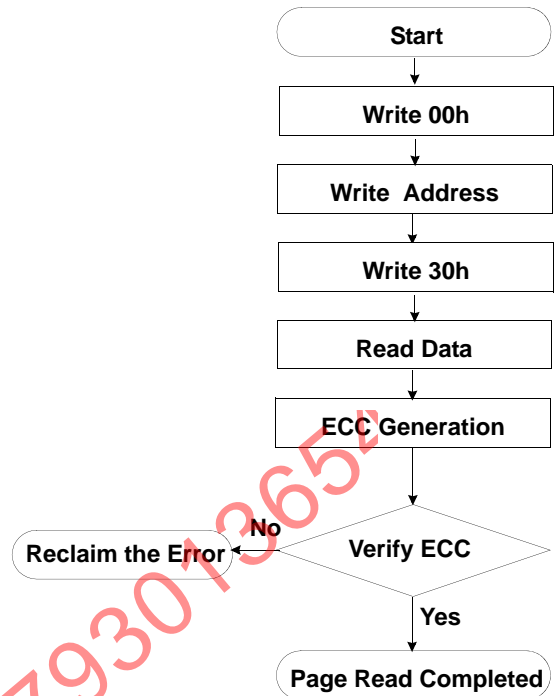
NAND Flash Technical Notes (Continued)

Erase Flow Chart

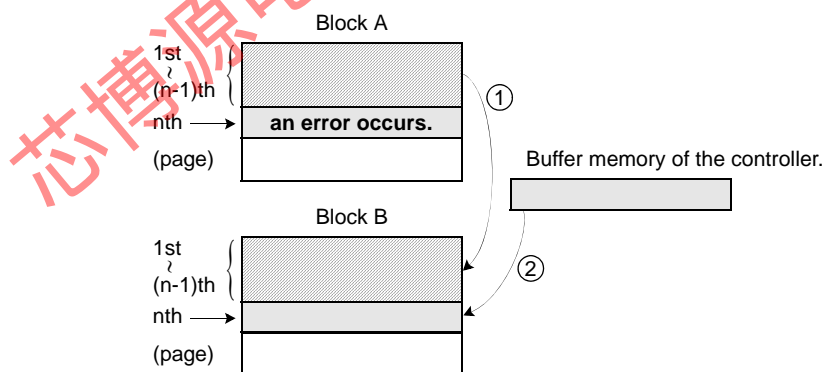


(*): If erase operation results in an error, map out the failing block and replace it with another block.

Read Flow Chart



Block Replacement



* Step1

When an error happens in the nth page of the Block 'A' during erase or program operation.

* Step2

Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')

* Step3

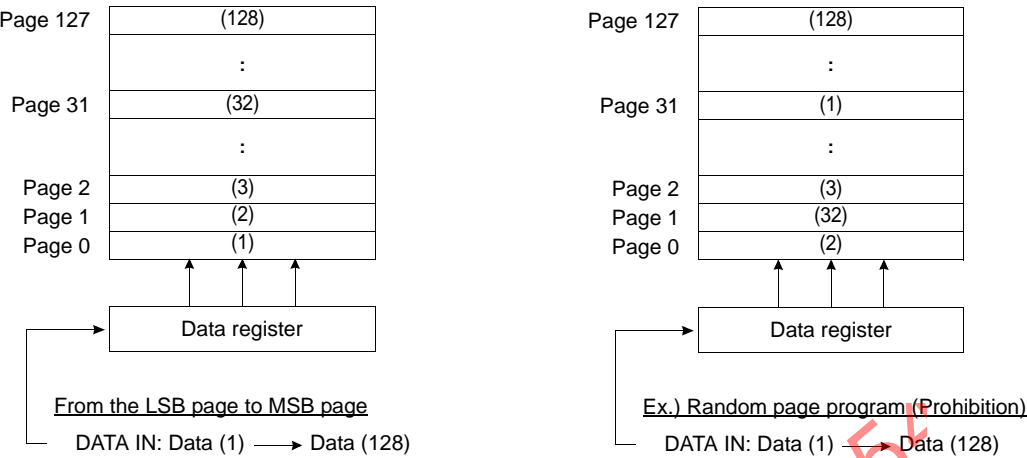
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.

* Step4

Do not erase or program Block 'A' by creating an 'invalid block' table or other appropriate scheme.

3.4 Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB doesn't need to be page 0.



Paired Page Address Information

Paired Page Address(1/2)		Paired Page Address(2/2)	
Group A	Group B	Group A	Group B
00h	02h	3Fh	42h
01h	04h	41h	44h
03h	06h	43h	46h
05h	08h	45h	48h
07h	0Ah	47h	4Ah
09h	0Ch	49h	4Ch
0Bh	0Eh	4Bh	4Eh
0Dh	10h	4Dh	50h
0Fh	12h	4Fh	52h
11h	14h	51h	54h
13h	16h	53h	56h
15h	18h	55h	58h
17h	1Ah	57h	5Ah
19h	1Ch	59h	5Ch
1Bh	1Eh	5Bh	5Eh
1Dh	20h	5Dh	60h
1Fh	22h	5Fh	62h
21h	24h	61h	64h
23h	26h	63h	66h
25h	28h	65h	68h
27h	2Ah	67h	6Ah
29h	2Ch	69h	6Ch
2Bh	2Eh	6Bh	6Eh
2Dh	30h	6Dh	70h
2Fh	32h	6Fh	72h
31h	34h	71h	74h
33h	36h	73h	76h
35h	38h	75h	78h
37h	3Ah	77h	7Ah
39h	3Ch	79h	7Ch
3Bh	3Eh	7Bh	7Eh
3Dh	40h	7Dh	7Fh

NOTE :

When program operation is abnormally aborted (ex. power-down, reset), not only page data under program but also paired page data may be damaged.

3.5 Interleaving operation

K9LBG08U0E and K9HCG08U1E devices are composed of two chips sharing per CE pin. They provide interleaving operation between two chips. This interleaving operation improves the system throughput almost twice compared to non-interleaving operation.

At first, the host issues a operation command to one of the LSB chips, say (chip #1). Due to DDP device goes into busy state. During this time, MSB chip (chip #2) is in ready state. So it can execute the operation command issued by the host.

After the execution of operation by LSB chip (chip #1), it can execute another operation regardless of MSB chip (chip #2). Before that the host needs to check the status of LSB chip (chip #1) by issuing F1h command. Only when the status of LSB chip (chip #1) becomes ready state, host can issue another operation command. If LSB chip (chip #1) is in busy state, the host has to wait for LSB chip (chip #1) to get into ready state.

Similarly, MSB chip (chip #2) can execute another operation after the completion of the previous operation. The host can monitor the status of MSB chip (chip #2) by issuing F2h command. When MSB chip (chip #2) shows ready state, host can issue another operation command to MSB chip (chip #2).

This interleaving algorithm improves the system throughput almost twice. The host can issue page operation command to each chip individually. This reduces the time lag for the completion of operation.

NOTES : During interleave operations, 70h command is prohibited.

[Table 2] F1h Read Status Register Definition

I/O No.	Page Program	Block Erase	Read	Definition
I/O 0	Chip1 Pass/Fail	Chip1 Pass/Fail	Not use	Pass : "0" Fail : "1"
I/O 1	Plane Pass/Fail	Plane Pass/Fail	Not use	Pass : "0" Fail : "1"
I/O 2	Not Use	Not Use	Not use	Don't -cared
I/O 3	Not Use	Not Use	Not Use	Don't -cared
I/O 4	Not Use	Not Use	Not Use	Don't -cared
I/O 5	Not Use	Not Use	Not Use	Don't -cared
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Protected : "0" Not Protected : "1"

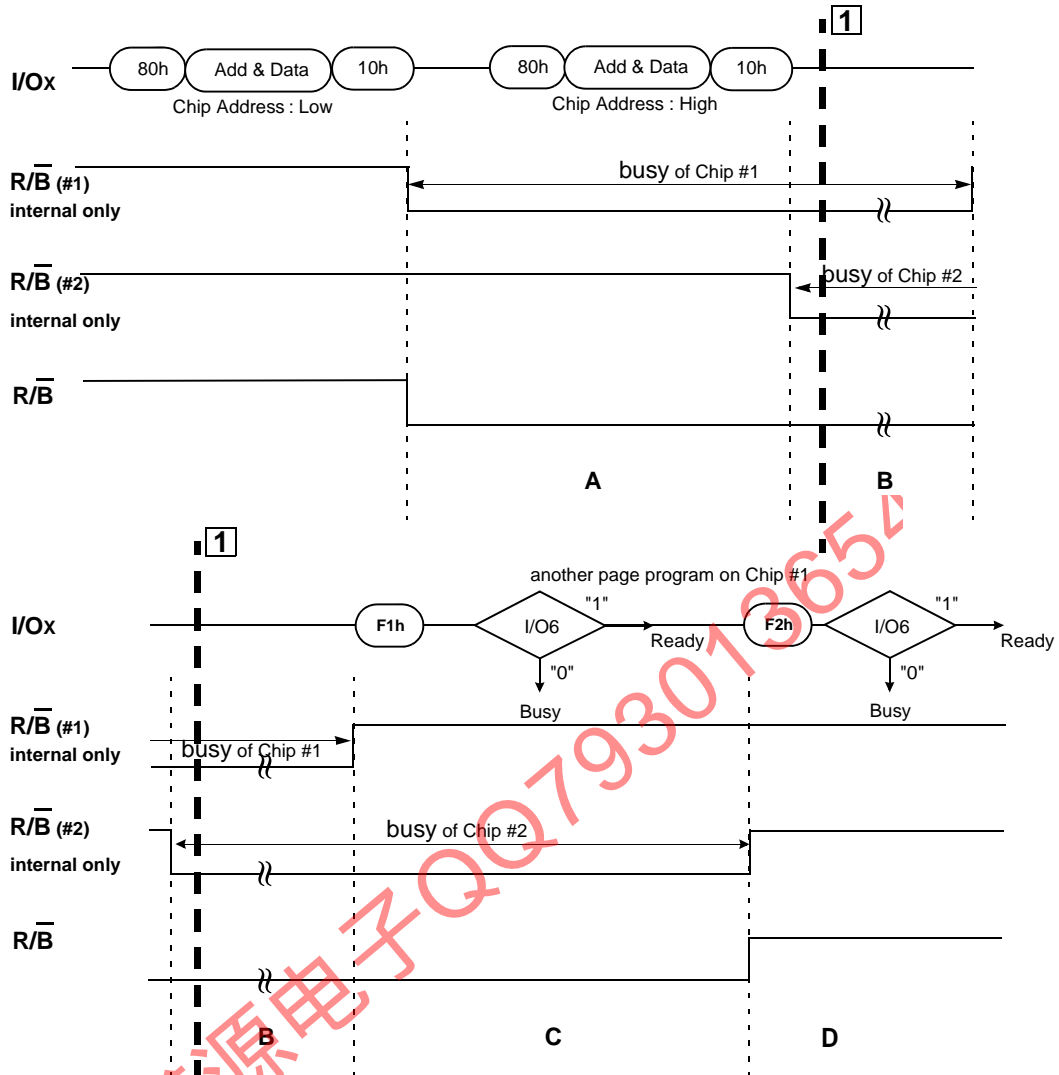
NOTE : 1. I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

[Table 3] F2h Read Status Register Definition

I/O No.	Page Program	Block Erase	Read	Definition
I/O 0	Chip2 Pass/Fail	Chip2 Pass/Fail	Not use	Pass : "0" Fail : "1"
I/O 1	Plane Pass/Fail	Plane Pass/Fail	Not use	Pass : "0" Fail : "1"
I/O 2	Not Use	Not Use	Not use	Don't -cared
I/O 3	Not Use	Not Use	Not Use	Don't -cared
I/O 4	Not Use	Not Use	Not Use	Don't -cared
I/O 5	Not Use	Not Use	Not Use	Don't -cared
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Protected : "0" Not Protected : "1"

NOTE : 1. I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

3.5.1 Interleaving Page Program



State A : Chip #1 is executing page program operation and chip #2 is in ready state. So the host can issue page program command to chip #2.

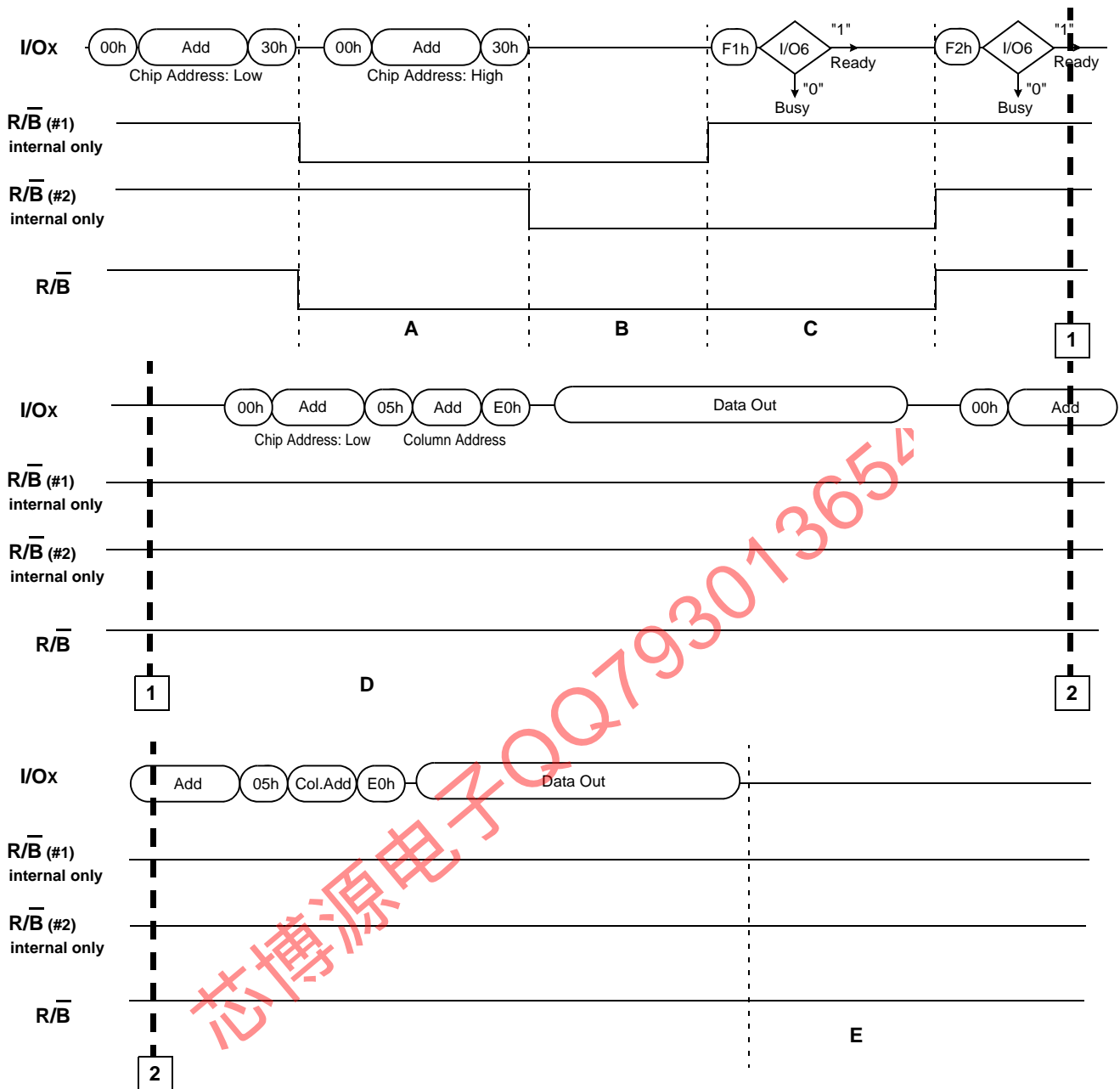
State B : Both chip #1 and chip #2 are executing page program operation.

State C : Page program on chip #1 is terminated, but page program on chip #2 is still operating. And the system should issue F1h /F2h command to detect the status of chip #1. If chip #1 is ready, status I/O6 is "1" and the system can issue another page program command to chip #1.

State D : Chip #1 and Chip #2 are ready.

According to the above process, the system can operate page program on chip #1 and chip #2 alternately.

3.5.2 Interleaving Page Read



State A : Chip #1 is executing page read operation, and chip #2 is in ready state. So the host can issue page read command to chip #2.

State B : Both chip #1 and chip #2 are executing page read operation.

State C : Page read on chip #1 is completed and chip #2 is still executing page read operation.

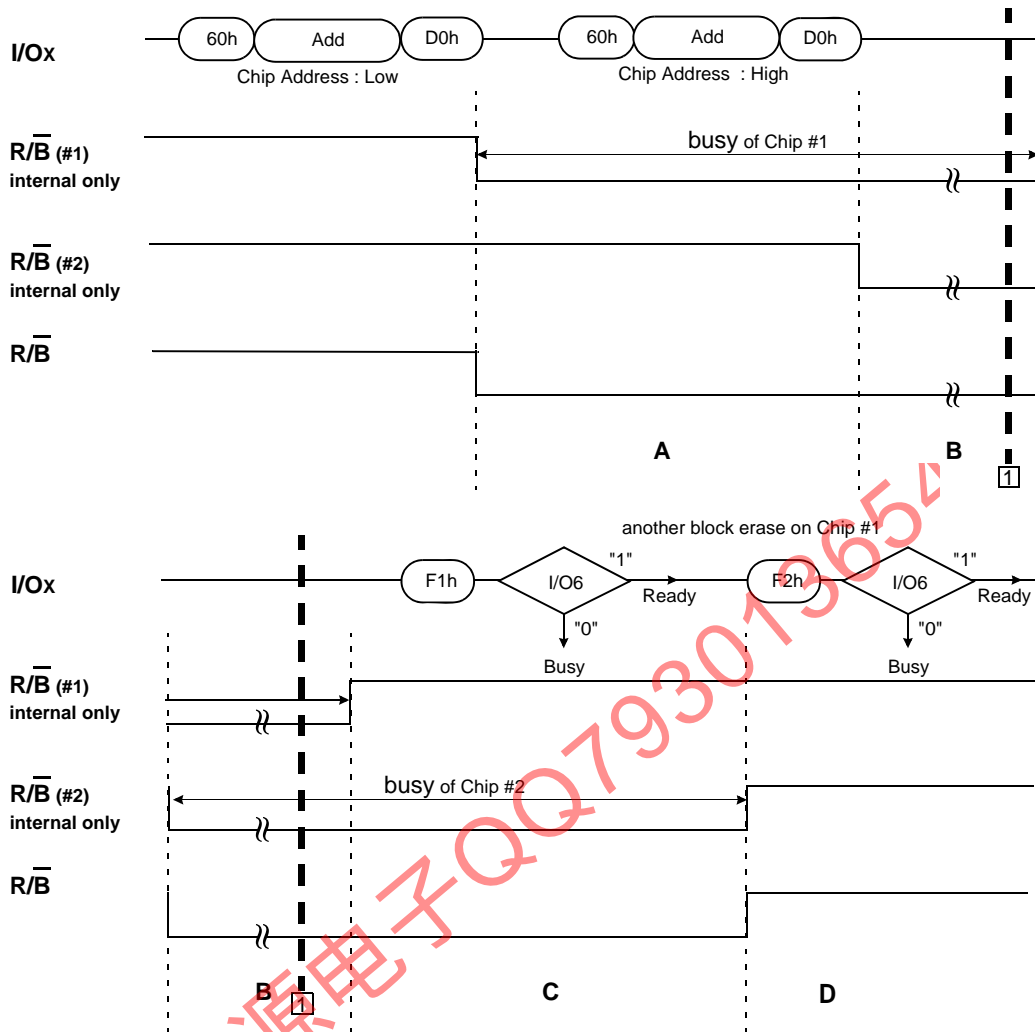
State D : Before the host read the data, the host should check the Ready/Busy status for both chips by F1h and F2h commands.

State E : Chip #1 and Chip #2 are ready.

Note : *F1h command is required to check the status of chip #1.

F2h command is required to check the status of chip #2.

3.5.3 Interleaving Block Erase



State A : Chip #1 is executing block erase operation, and chip #2 is in ready state. So the host can issue block erase command to chip #2.

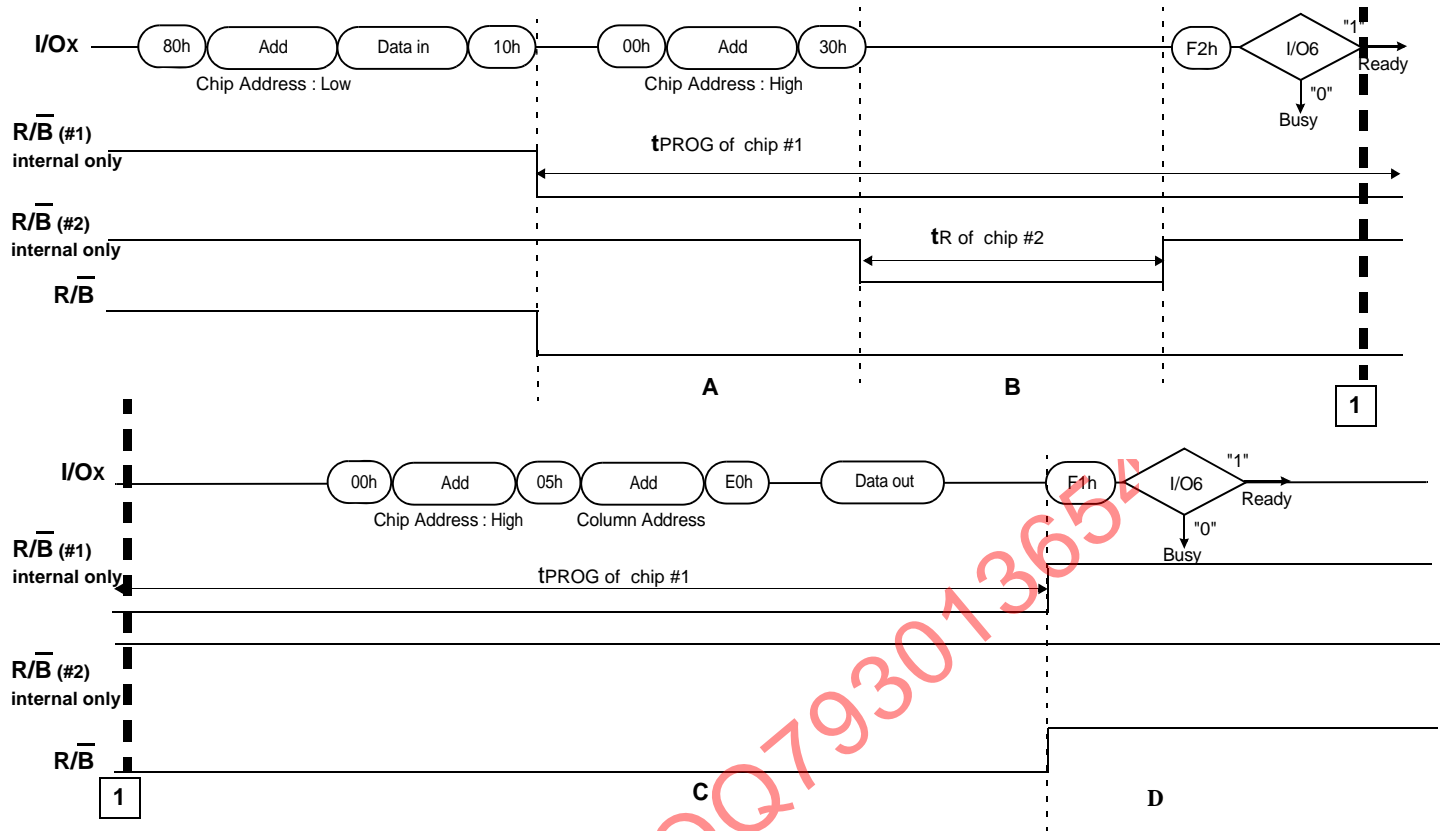
State B : Both chip #1 and chip #2 are executing block erase operation.

State C : Block erase on chip #1 is terminated, but block erase on chip #2 is still operating. And the system should issue F1h /F2h command to detect the status of chip #1. If chip #1 is ready, status I/O6 is "1" and the system can issue another block erase command to chip #1.

State D : Chip #1 and Chip #2 are ready.

According to the above process, the system can operate block erase on chip #1 and chip #2 alternately.

3.5.4 Interleaving Read to Page Program



State A : Chip #1 is executing page program operation, and chip #2 is in ready state. So the host can issue read command to chip #2.

State B : Both chip #1 is executing page program operation and chip #2 is executing read operation.

State C : Read operation on chip #2 is completed and chip #2 is ready for the next operation. Chip #1 is still executing page program operation.

State D : Both chip #1 and chip #2 are ready.

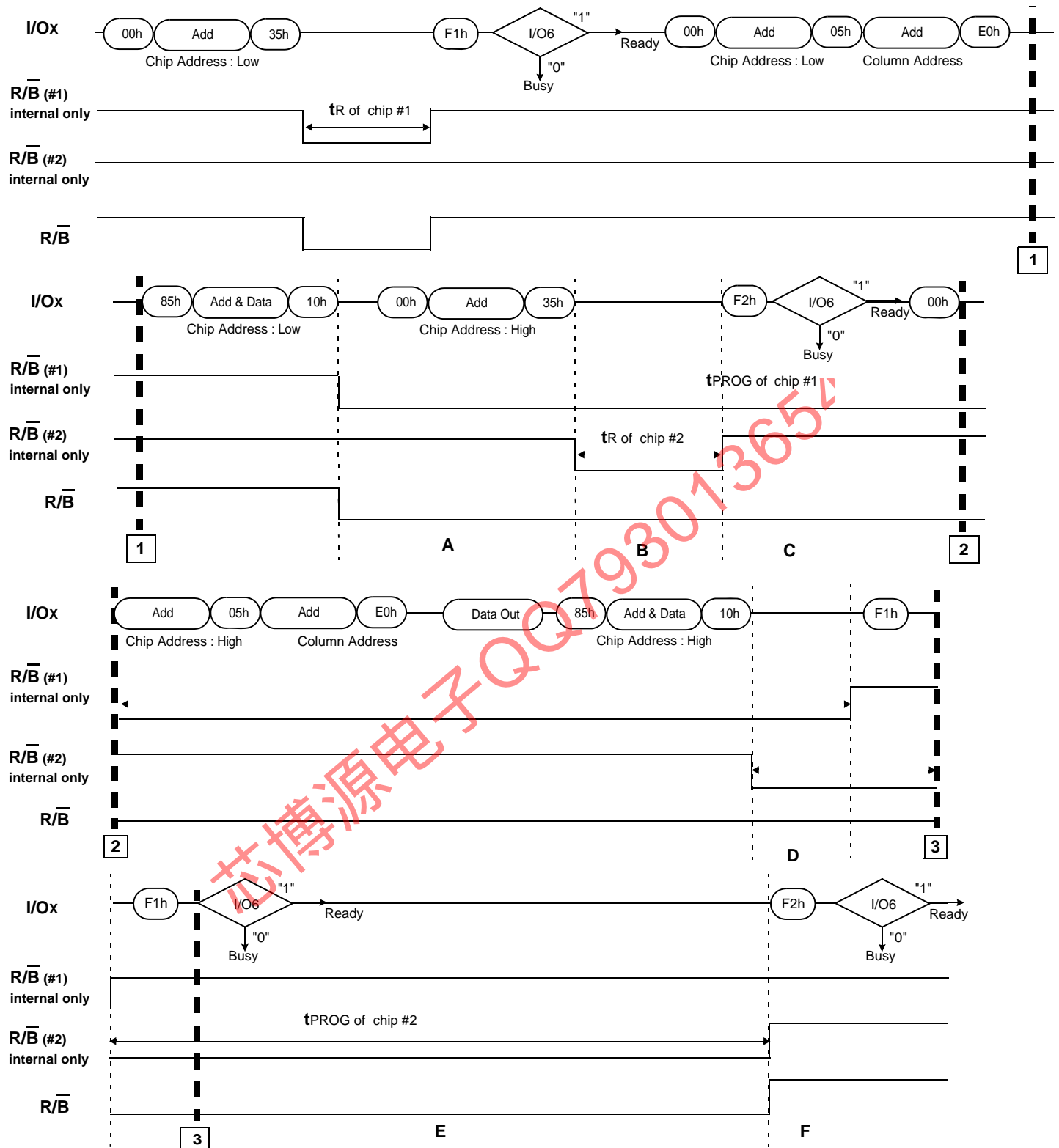
Note :

*F1h command is required to check the status of chip #1 to issue the next command to chip #1.

F2h command is required to check the status of chip #2 to issue the next command to chip #2.

As the above process, the system can operate Interleave read to page program on chip #1 and chip #2 alternatively.

3.5.5 Interleaving Copy-Back Program



State A : Chip #1 is executing copy-back program operation, and chip #2 is in ready state. So the host can issue read for copy-back command to chip #2.

State B : Chip #1 is executing copy-back program operation and chip #2 is executing read for copy-back operation.

State C : Read for copy-back operation on chip #2 is completed and chip #2 is ready for the next operation. Chip #1 is still executing copy-back program operation.

State D : Both chip #1 and chip #2 are executing copy-back program operation.

State E : Chip #2 is still executing a copy-back program operation, and chip #1 is in ready for the next operation.

State F : Both chip #1 and chip #2 are ready.

Note :

*F1h command is required to check the status of chip #1 to issue the next command to chip #1.

*F2h command is required to check the status of chip #2 to issue the next command to chip #2.

As the above process, the system can operate Interleave copy-back program on chip #1 and chip #2 alternatively.

3.6 System Interface Using $\overline{\text{CE}}$ don't-care.

For an easier system interface, $\overline{\text{CE}}$ may be inactive during the data-loading or serial access as shown below. The internal 8,628byte data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of μ -seconds, de-activating $\overline{\text{CE}}$ during the data-loading and serial access would provide significant savings in power consumption.

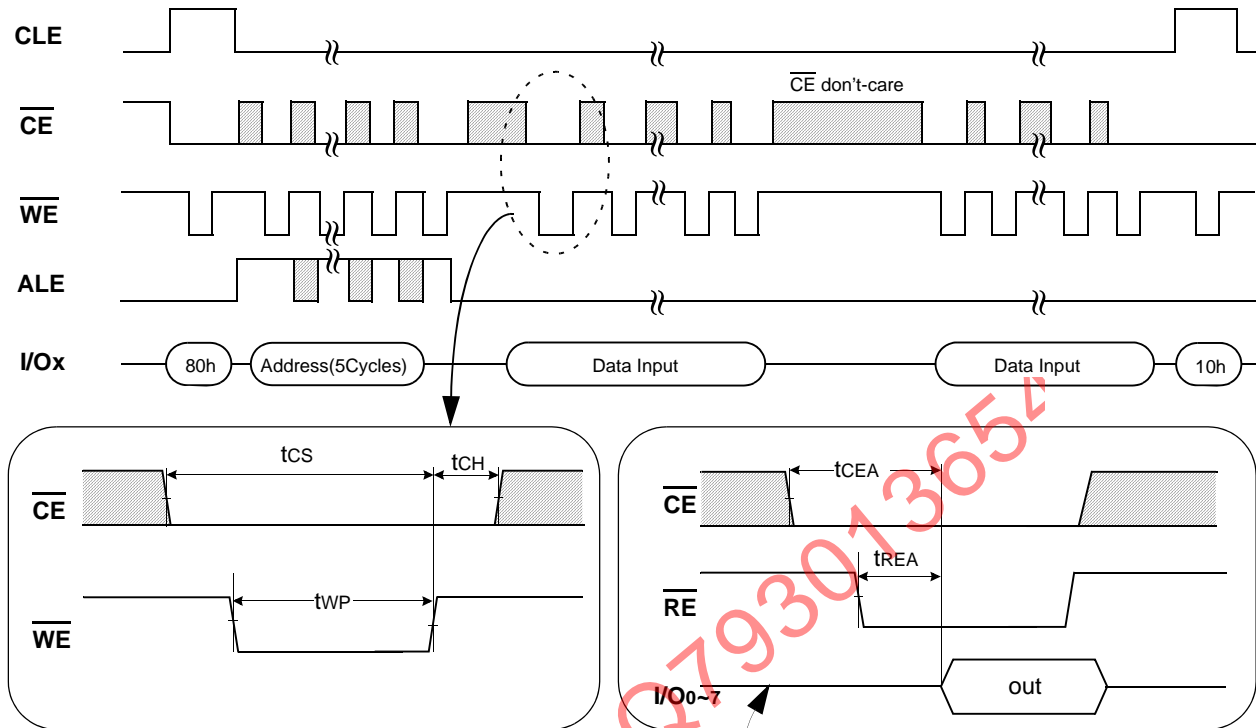


Figure 4. Program Operation with $\overline{\text{CE}}$ don't-care.

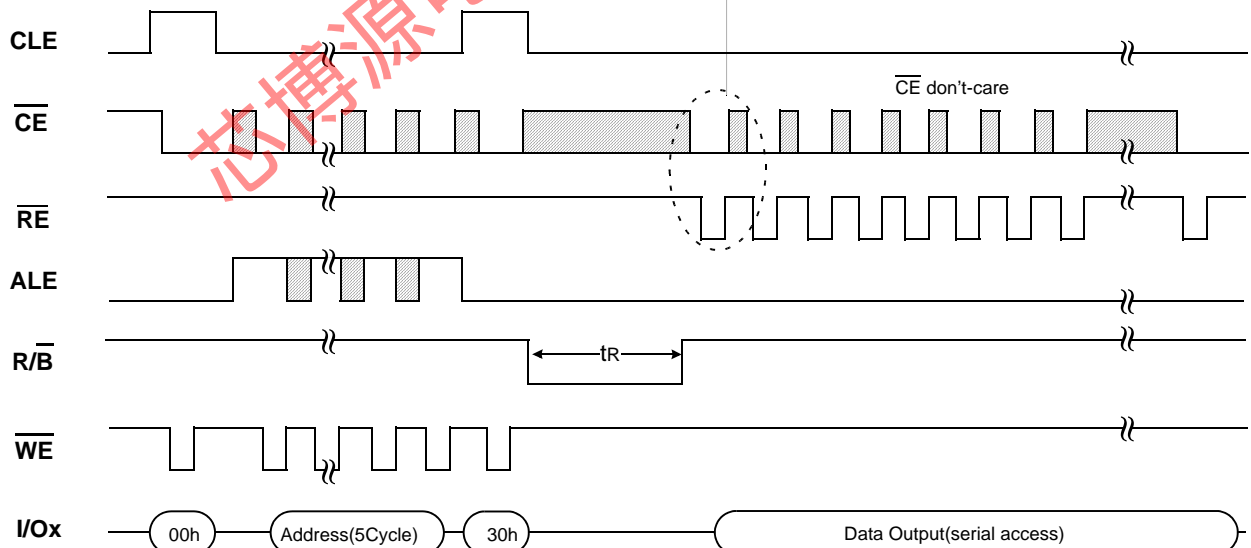
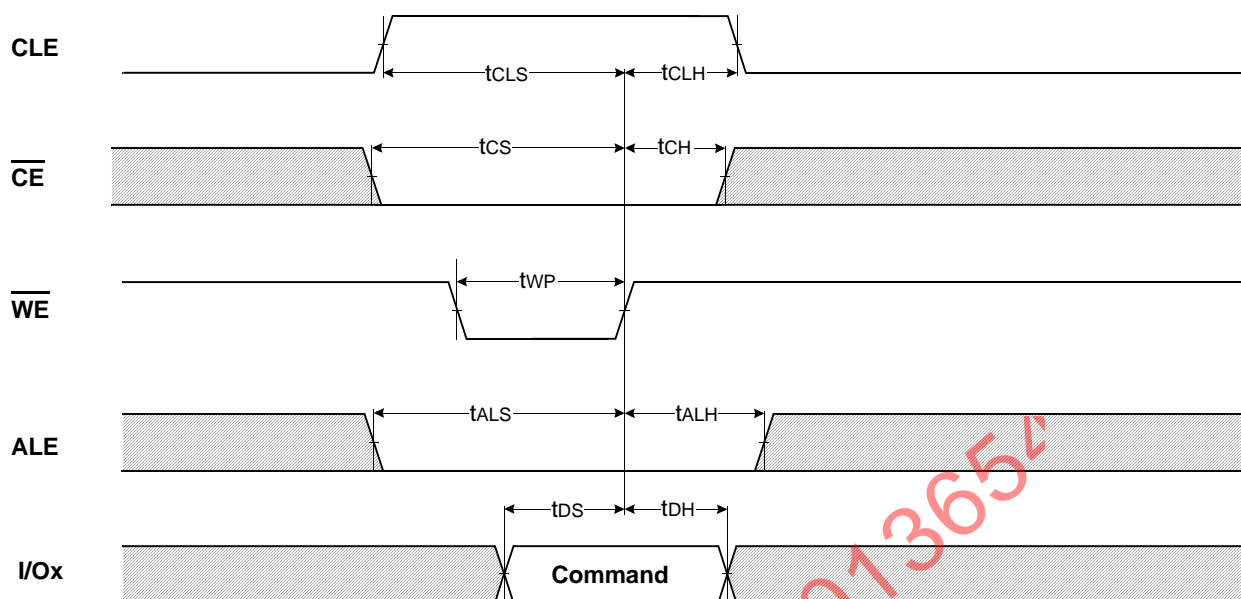


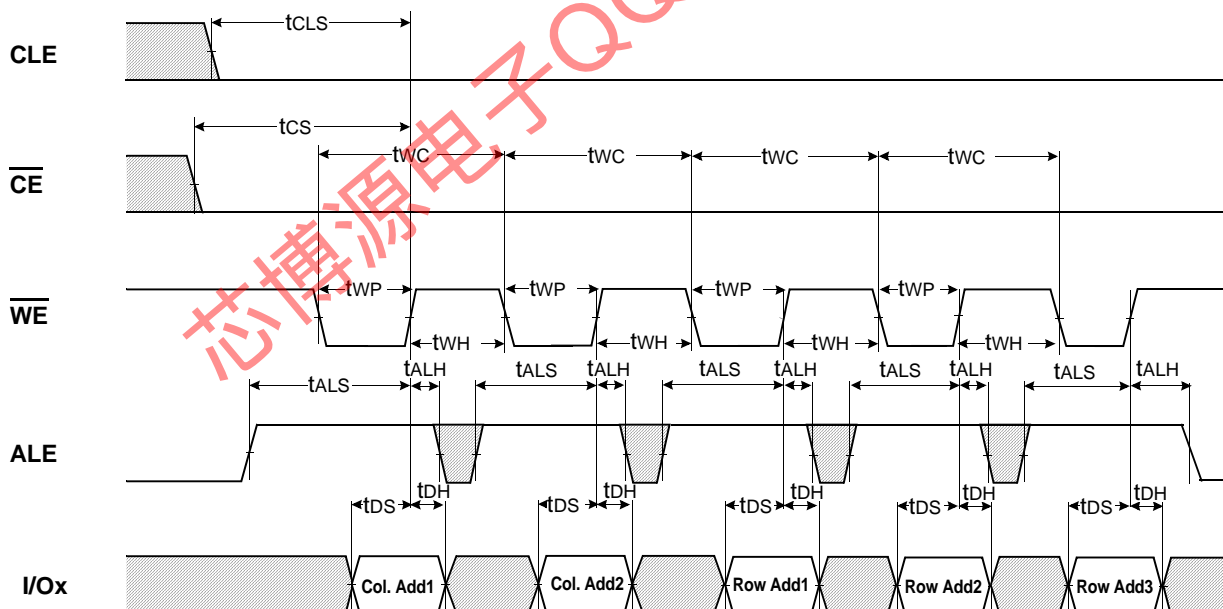
Figure 5. Read Operation with $\overline{\text{CE}}$ don't-care.

4.0 TIMING DIAGRAMS

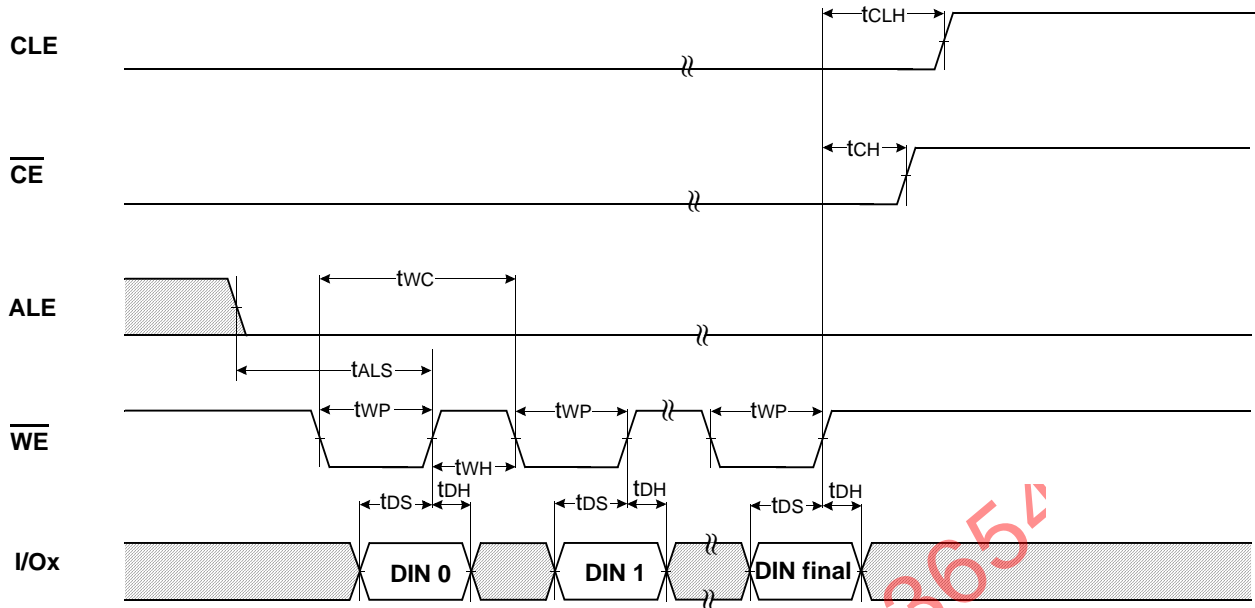
4.1 Command Latch Cycle



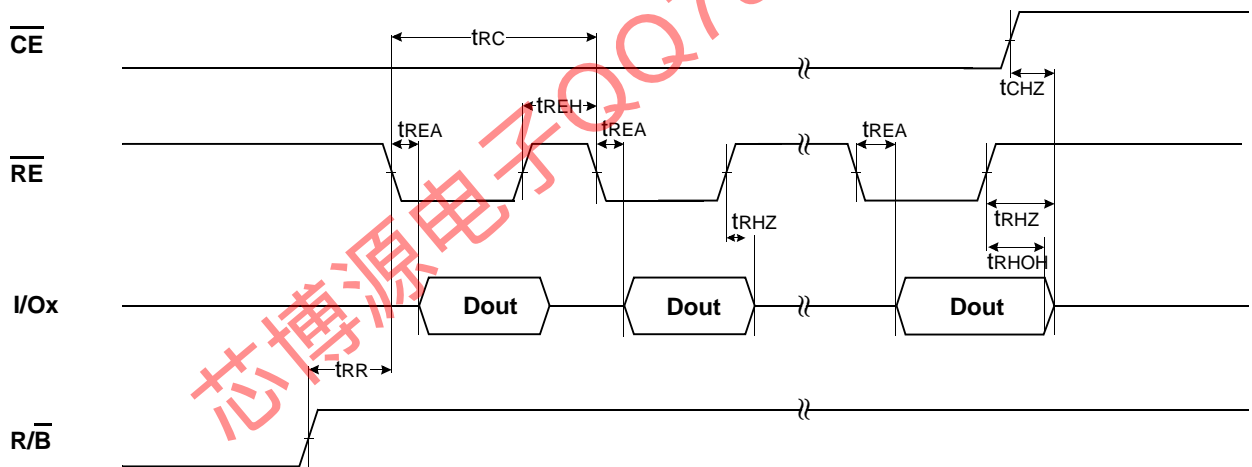
4.2 Address Latch Cycle



4.3 Input Data Latch Cycle



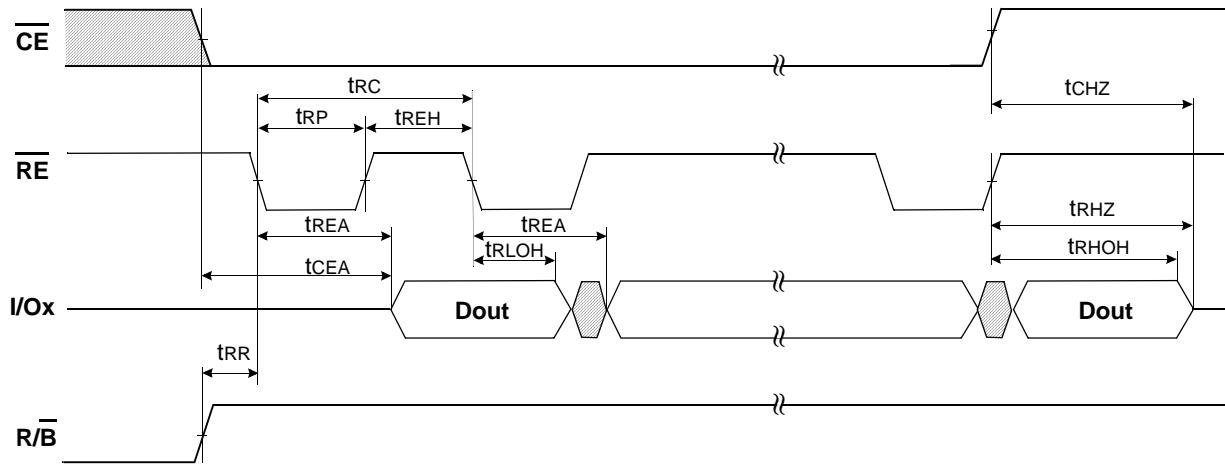
4.4 * Serial Access Cycle after Read (CLE=L, WE=H, ALE=L)



NOTES :

- 1) Transition is measured at $\pm 200\text{mV}$ from steady state voltage with load.
This parameter is sampled and not 100% tested.
- 2) t_{RLOH} is valid when frequency is higher than 20MHz.
 t_{RHOH} starts to be valid when frequency is lower than 20MHz.

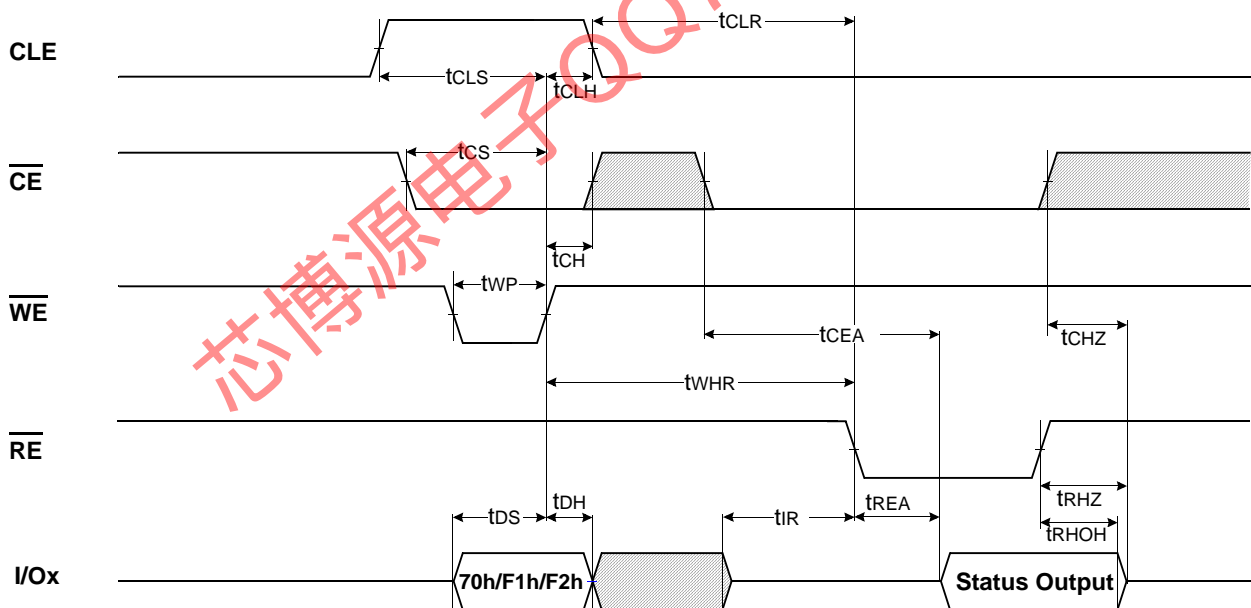
4.5 Serial Access Cycle after Read(EDO Type, CLE=L, \overline{WE} =H, ALE=L)



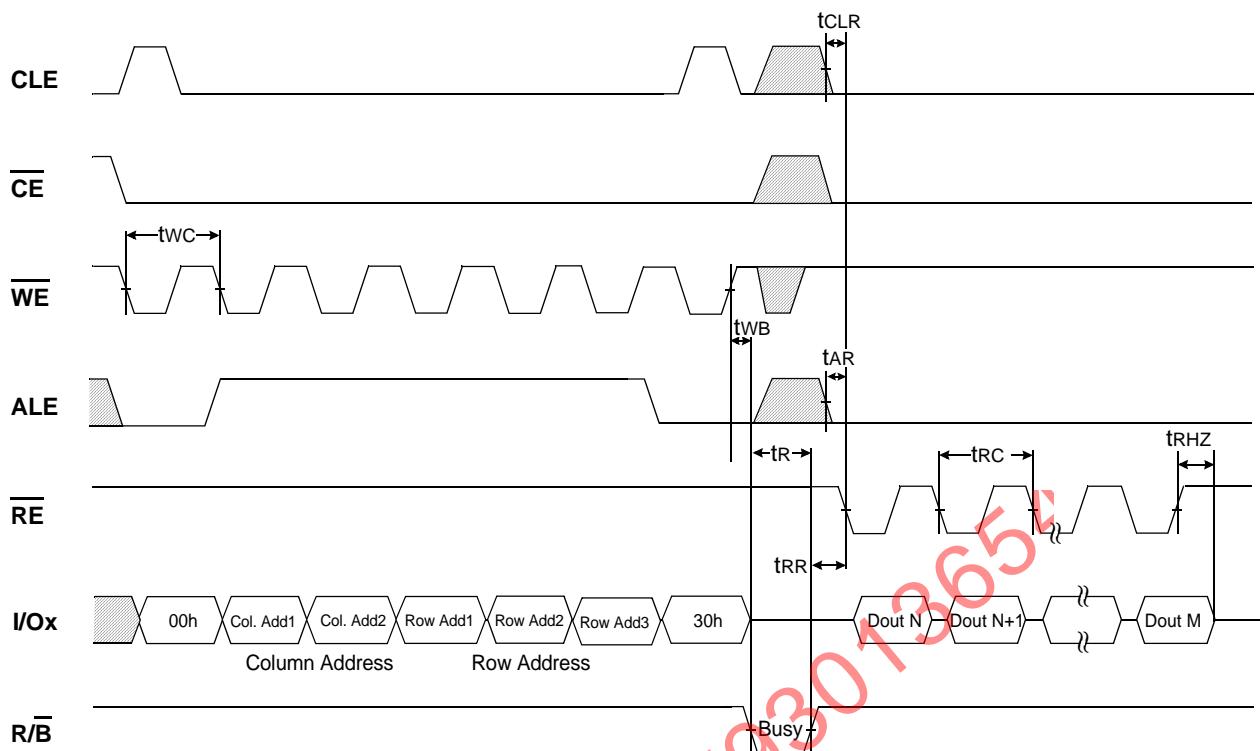
NOTES :

- 1) Transition is measured at $\pm 200\text{mV}$ from steady state voltage with load.
This parameter is sampled and not 100% tested.
- 2) t_{RLOH} is valid when frequency is higher than 20MHz.
 t_{RHOH} starts to be valid when frequency is lower than 20MHz.

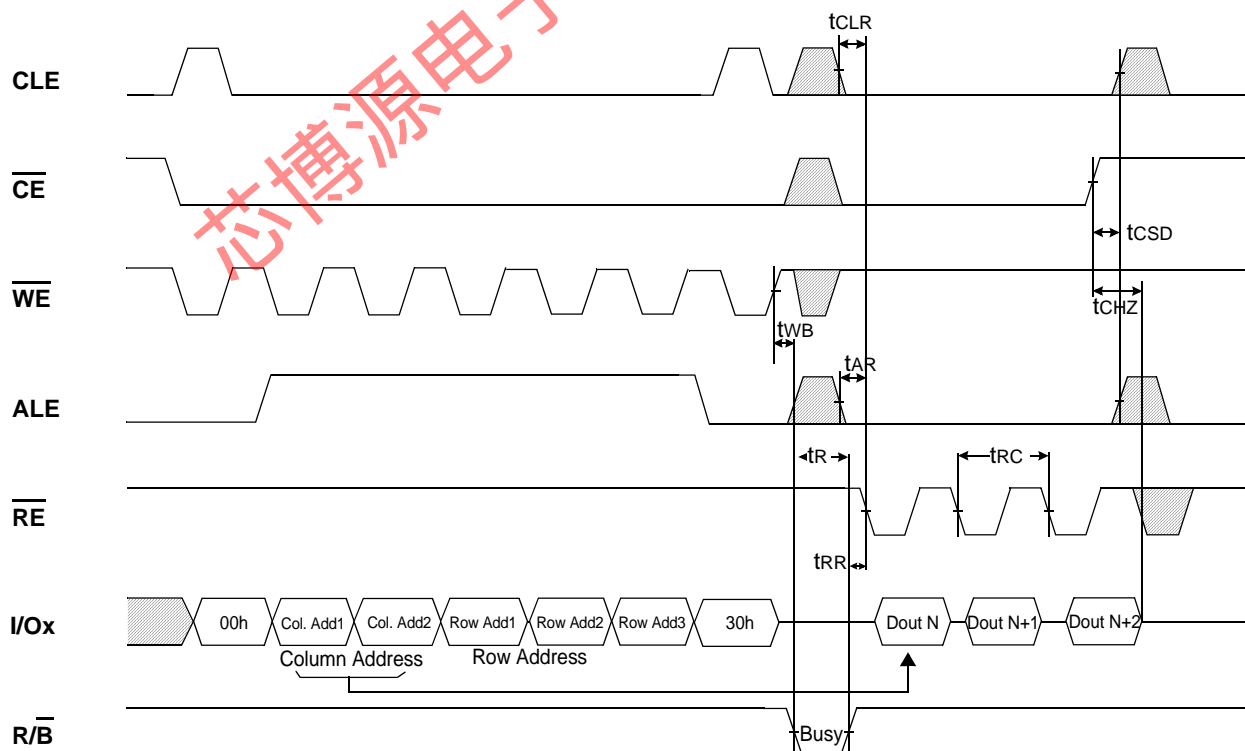
4.6 Status Read Cycle



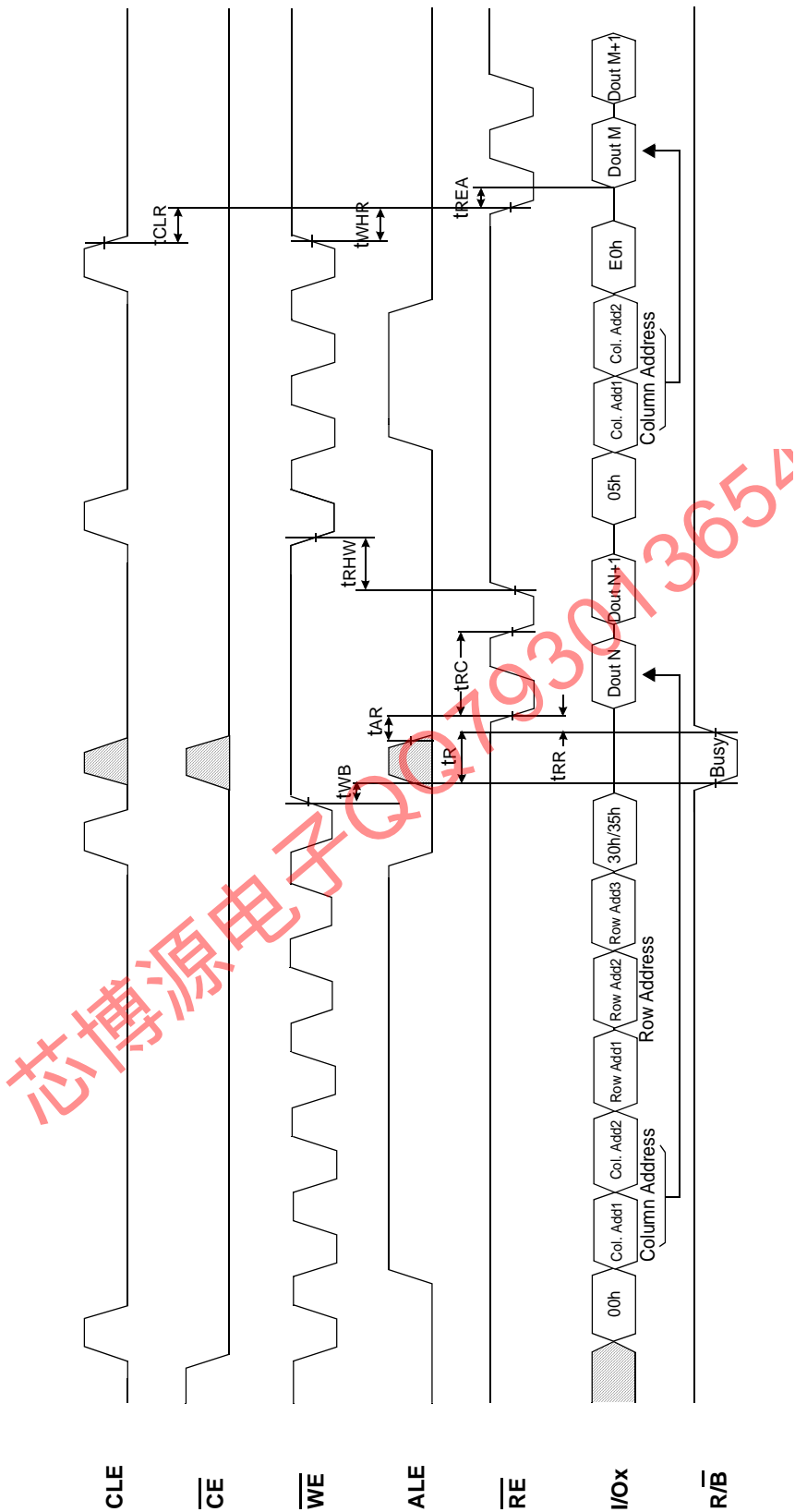
4.7 Read Operation



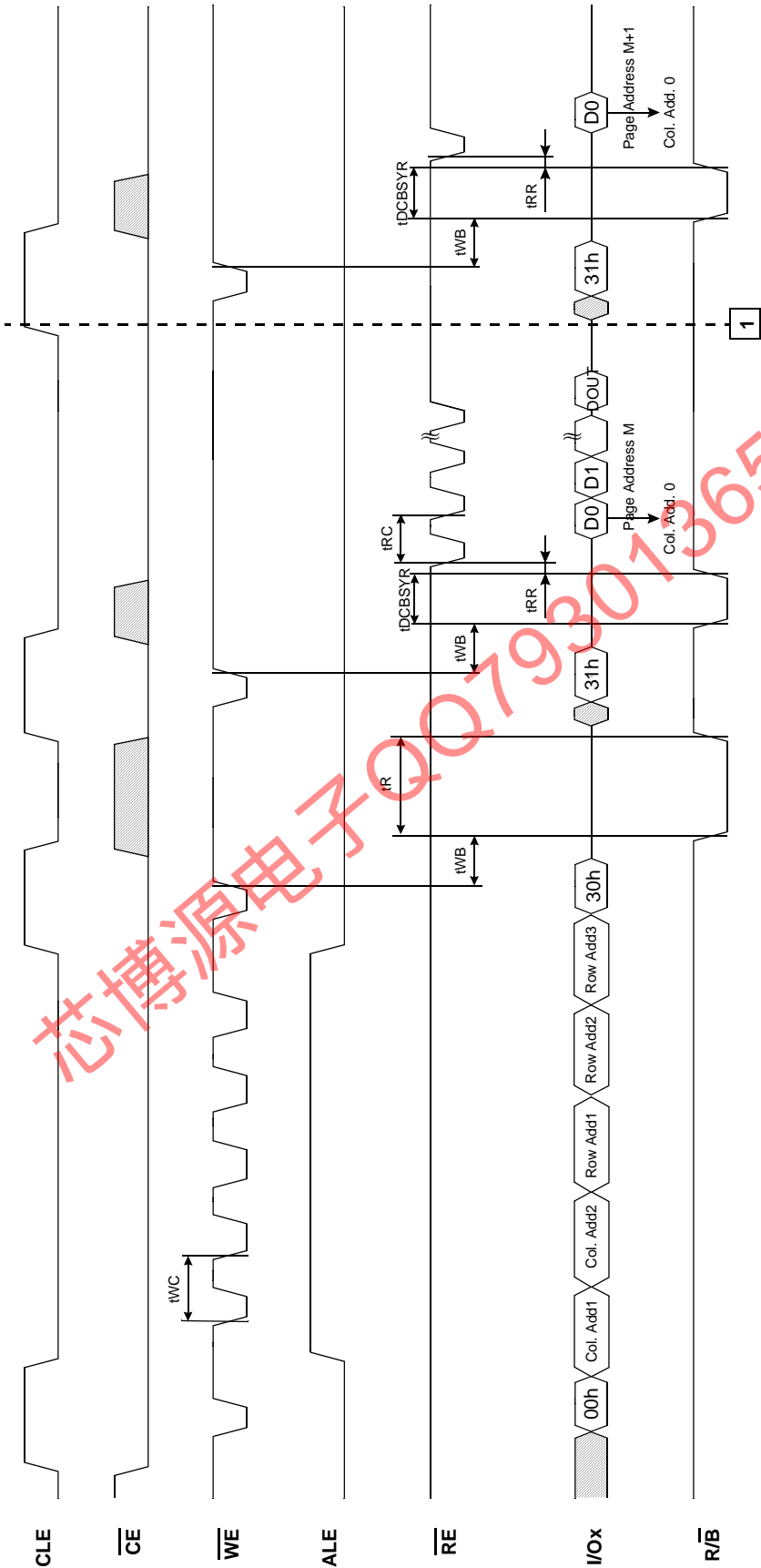
4.8 Read Operation(Intercepted by $\overline{\text{CE}}$)



4.9 Random Data Output In a Page

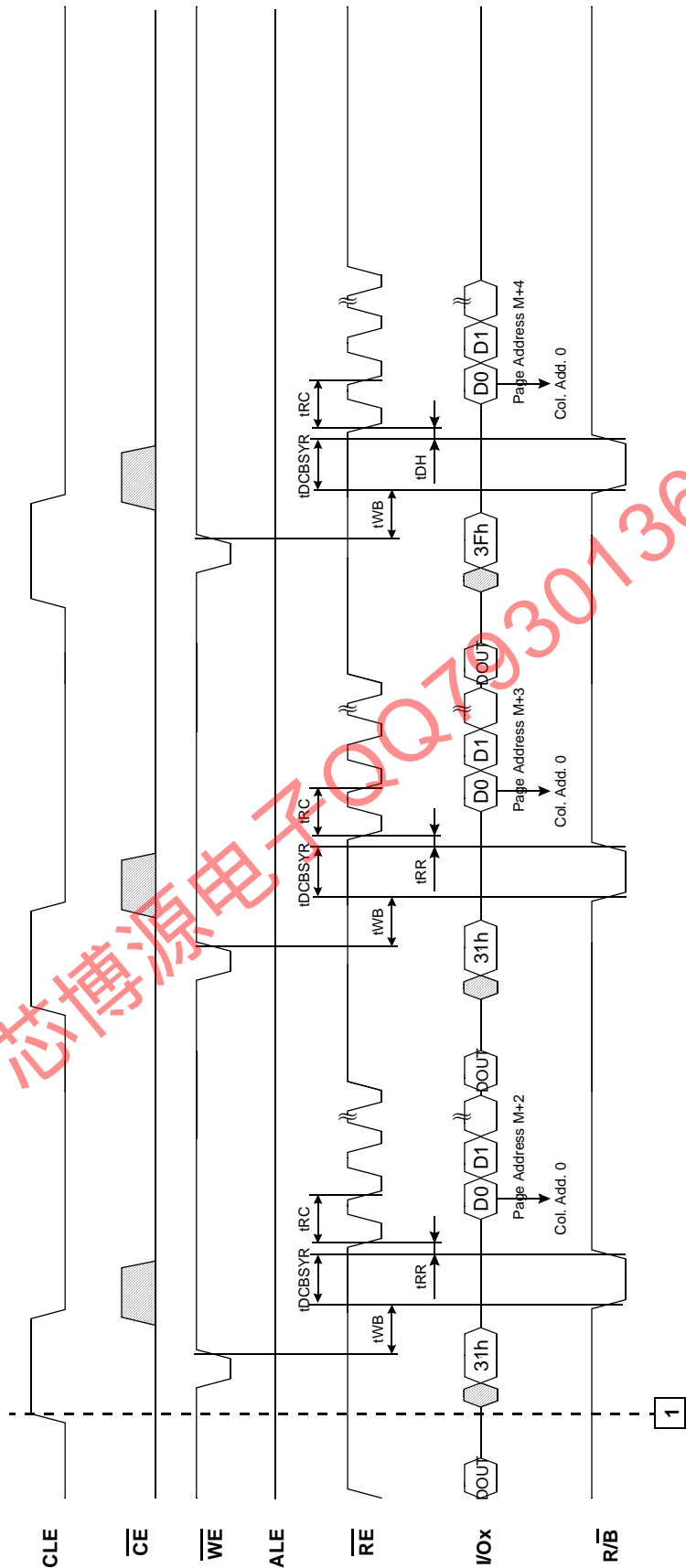


4.10 Cache Read Operation(1/2)



NOTE : 1. The column address will be reset to 0 by the 31h command input.
2. Cache Read operation is available only within a block.

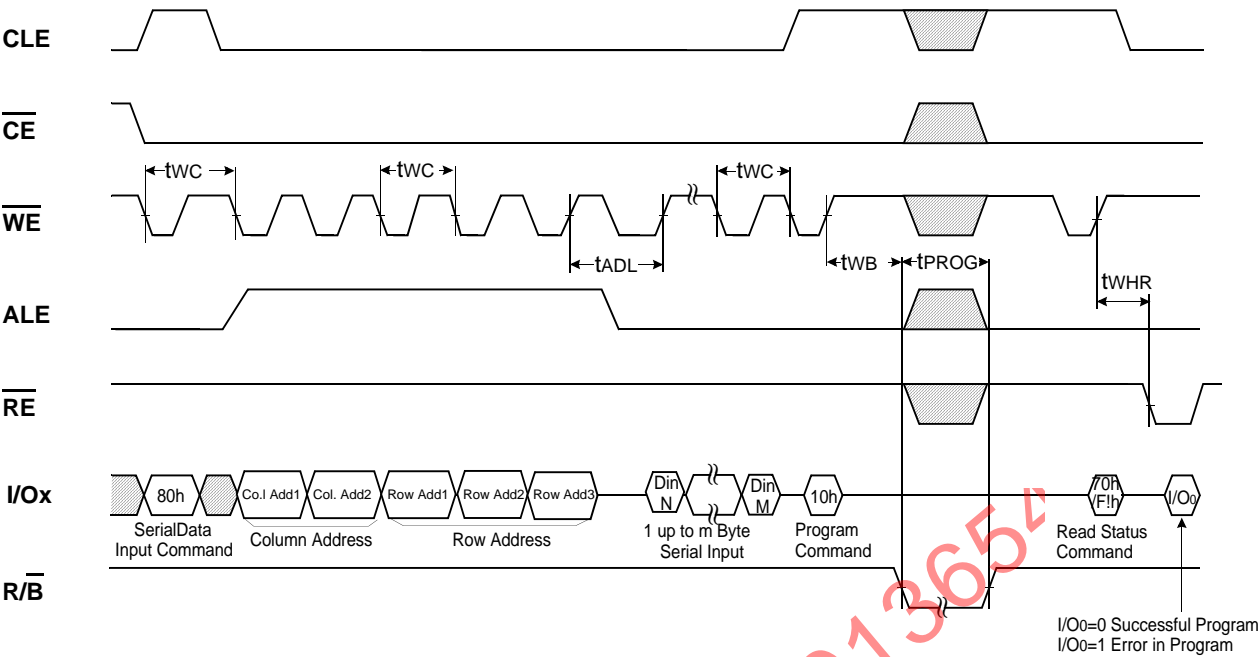
4.11 Cache Read Operation(2/2)



NOTE : 1. The column address will be reset to 0 by the 31h and 3Fh command input.
2. Cache Read operation is available only within a block.

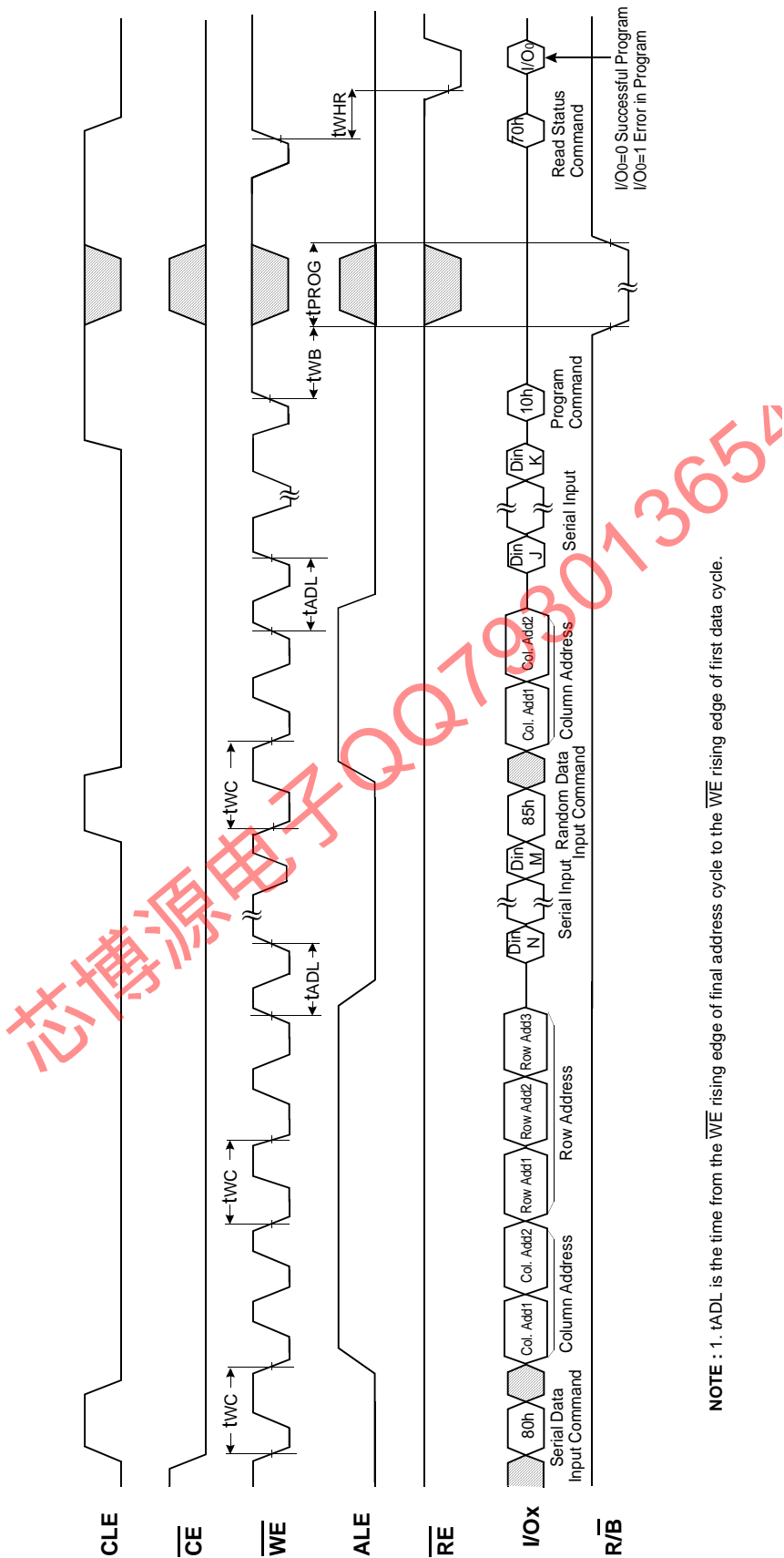


4.12 Page Program Operation



NOTE :
 t_{ADL} is the time from the \overline{WE} rising edge of final address cycle to the \overline{WE} rising edge of first data cycle.

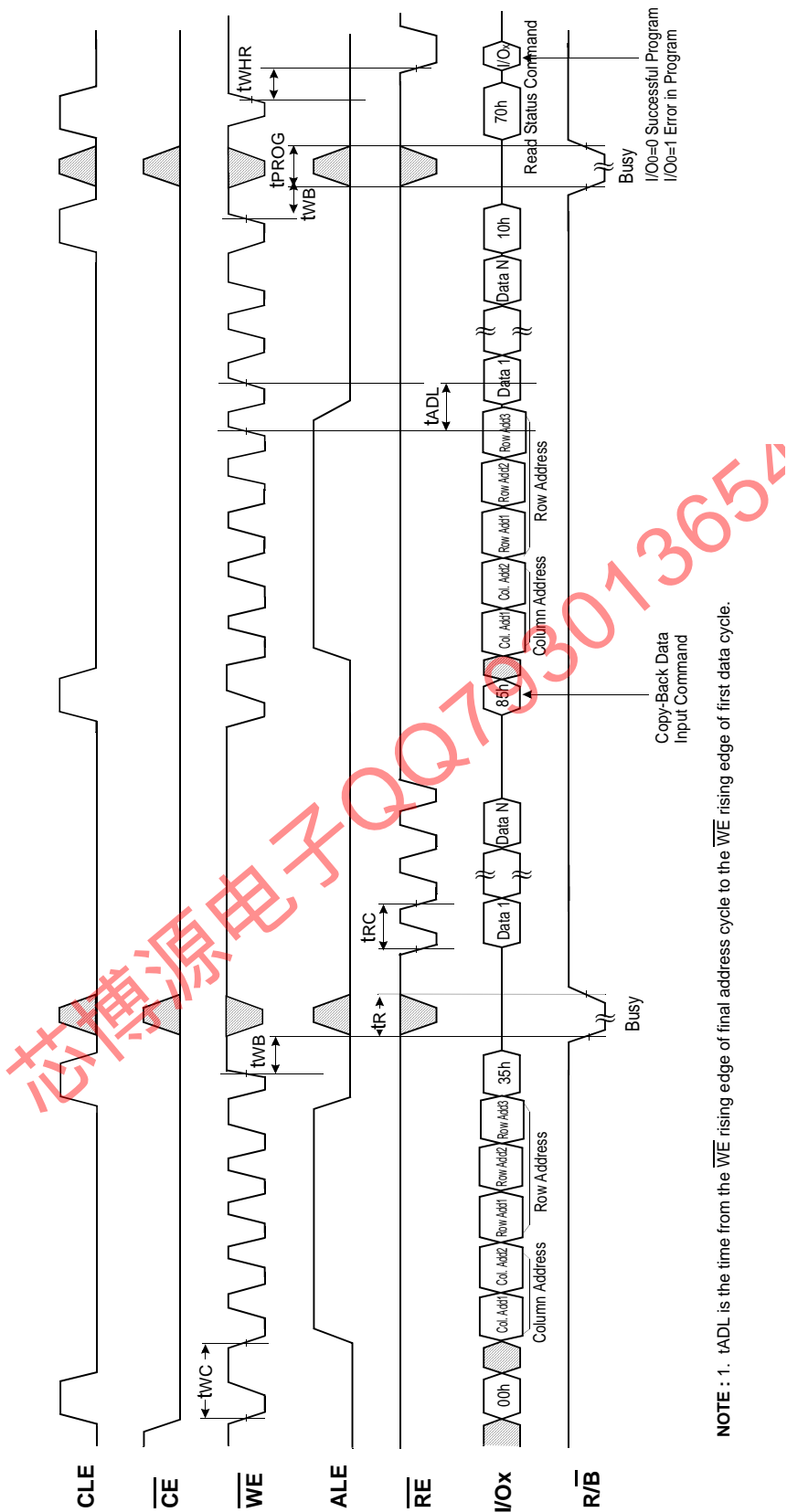
4.13 Page Program Operation with Random Data Input



NOTE : 1. tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.



4.14 Copy-Back Program Operation with Random Data Input



The diagram shows the timing relationship between control signals and data/address inputs for the Program Confirm Command (True). The signals involved are CLE, CE, WE, ALE, RE, I/Ox, and R/B. The data bus (I/Ox) carries the following sequence of information:

- Serial Data**: 80h
- Column Address**: Col. Add0, Col. Add1, Col. Add2
- Row Address**: Row Add0, Row Add1, Row Add2
- Data Input**: D[7:N], D[M:M]
- Program Command (Dummy)**: 15h
- Program Confirm Command (True)**

Key timing parameters shown include:

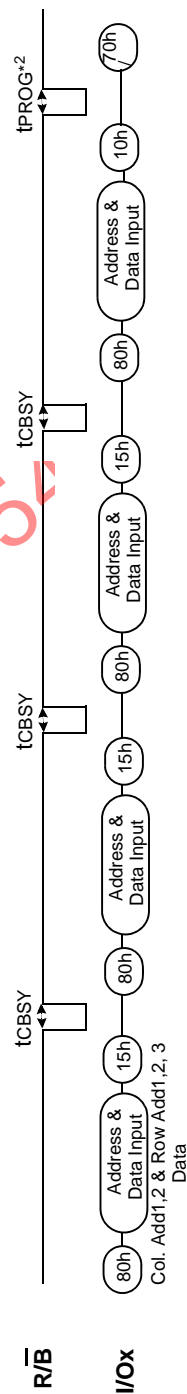
- tWC: Write Cycle time from WE to start of data input.
- tCASY: CAS latency from CE to start of data input.
- tWB: Write Buffer delay from WE to start of data input.
- tADL: Access Delay Latency from ALE to start of data input.
- tIOP: Input Output Pulse width from I/Ox signal transition.

The diagram also indicates that the sequence can be repeated up to 127 times (Max. 127 times repeatable).

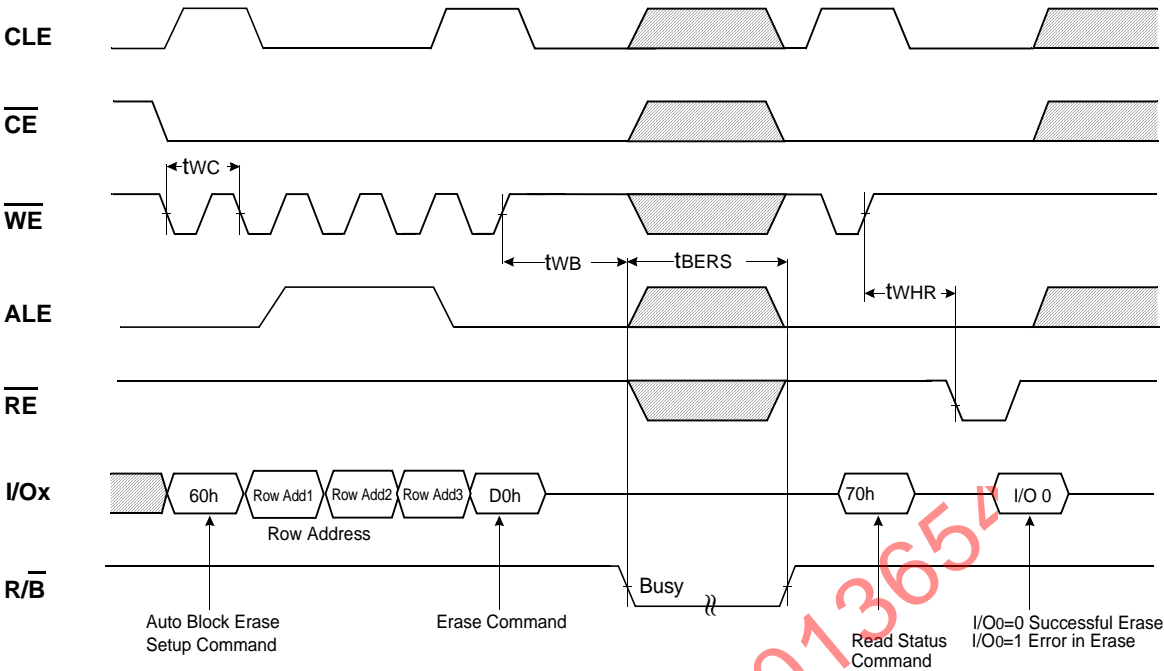
NOTE : 1. t_{ADL} is the time from the \overline{WE} rising edge of final address cycle to the \overline{WE} rising edge of first data cycle.
2. Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula.

$t_{\text{PROG}} = \text{Program time for the last page} + \text{Program time for the (last - 1)}^{\text{th}} \text{ page}$
 $- (\text{command input cycle time} + \text{address input cycle time} + \text{Last page data loading time})$

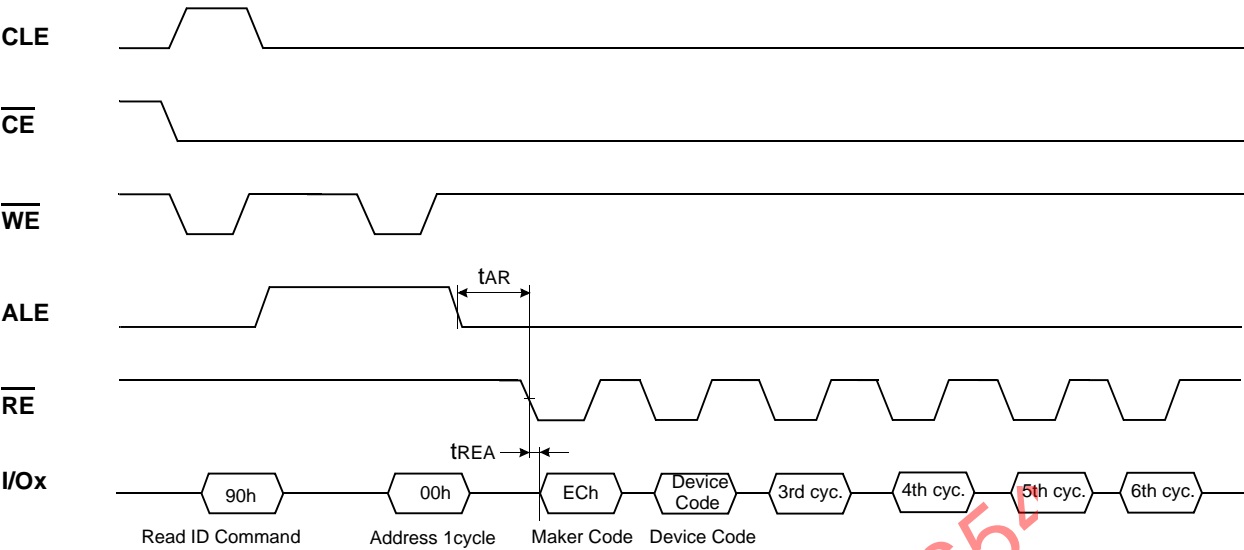
Ex.) Cache Program



4.16 Block Erase Operation



4.17 Read ID Operation



Device	Device Code (2nd Cycle)	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
K9GAG08U0E	D5h	84h	72h	50h	42h
K9LBG08U0E	D7h	C5h		54h	
K9HCG08U1E					



4.17.1 ID Definition Table

	Description
1 st Byte	Maker Code
2 nd Byte	Device Code
3 rd Byte	Internal Chip Number, Cell Type, Number of Simultaneously Programmed Pages, Etc.
4 th Byte	Page Size, Block Size, Redundant Area Size.
5 th Byte	Plane Number, ECC Level, Organization.
6 th Byte	Device Technology, EDO, Interface.

3rd ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 Level Cell					0	0		
	4 Level Cell					0	1		
	8 Level Cell					1	0		
	16 Level Cell					1	1		
Number of Simultaneously Programmed Pages	1			0	0				
	2			0	1				
	4			1	0				
	8			1	1				
Interleave Operation Between multiple chips	Not Support		0						
	Support		1						
Cache Operation	Not Support	0							
	Support	1							

4th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (w/o redundant area)	2KB							0	0
	4KB							0	1
	8KB							1	0
	Reserved							1	1
Block Size (w/o redundant area)	128KB	0		0	0				
	256KB	0		0	1				
	512KB	0		1	0				
	1MB	0		1	1				
	Reserved	1		0	0				
	Reserved	1		0	1				
	Reserved	1		1	0				
	Reserved	1		1	1				
Redundant Area Size (byte / Page Size)	Reserved		0			0	0		
	128B		0			0	1		
	218B		0			1	0		
	400B		0			1	1		
	436B		1			0	0		
	Reserved		1			0	1		
	Reserved		1			1	0		
	Reserved		1			1	1		

5th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Plane Number	1					0	0		
	2					0	1		
	4					1	0		
	8					1	1		
ECC Level	1bit / 512B		0	0	0				
	2bit / 512B		0	0	1				
	4bit / 512B		0	1	0				
	8bit / 512B		0	1	1				
	16bit / 512B		1	0	0				
	24bit / 1KB		1	0	1				
	Reserved		1	1	0				
	Reserved		1	1	1				
Reserved		0						0	0

6th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Device Version	50nm						0	0	0
	40nm						0	0	1
	30nm						0	1	0
	Reserved						0	1	1
	Reserved						1	0	0
	Reserved						1	0	1
	Reserved						1	1	0
	Reserved						1	1	0
EDO	Not Support		0						
	Support		1						
Interface	SDR	0							
	DDR	1							
Reserved				0	0	0			

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5.0 DEVICE OPERATION

5.1 Page Read

Page read is initiated by writing 00h-30h to the command register along with five address cycles. The 8,628 bytes of data within the selected page are transferred to the cache registers via data registers in less than 400μs(t_R). The system controller can detect the completion of this data transfer(t_R) by analyzing the output of R/B pin. Once the data in a page is loaded into the cache registers, they may be read out in 30ns cycle time by sequentially pulsing RE. The repetitive high to low transitions of the RE clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

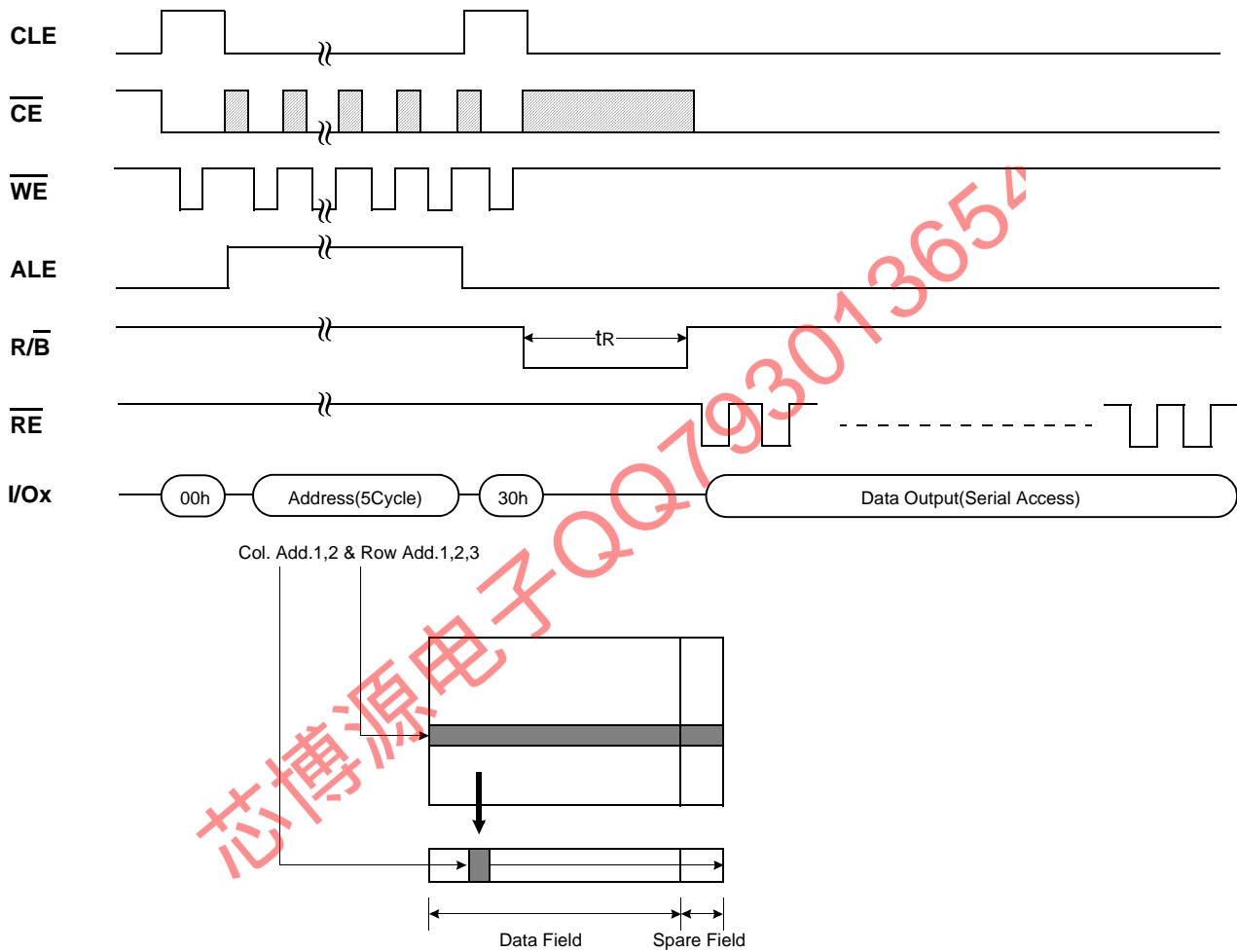


Figure 6. Read Operation

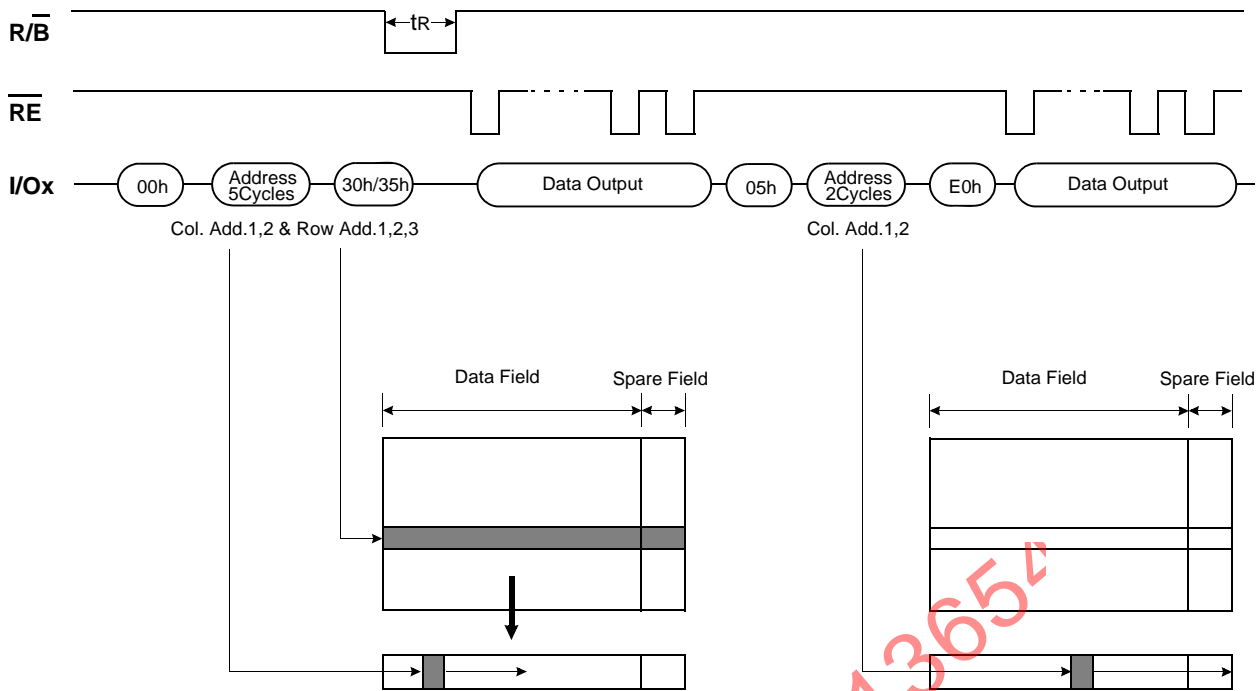


Figure 7. Random Data Output In a Page

5.2 CACHE READ

Cache Read is an extension of Page Read, which is executed with 8,628byte data registers, and is available only within a block. Since the device has 1 page of cache memory, serial data output may be executed while data in the memory cell is read into data registers.

Cache read is also initiated by writing 00h-30h to the command register along with five address cycles. After initial power up, 00h command is latched. Therefore only five address cycles and 30h command initiates that operation after initial power up. The 8,628 bytes of data within the selected page are transferred to the cache registers via data registers in less than 400 μ s(t_R). After issuing Cache Read command(31h), read data in the data registers is transferred to cache registers for a short period of time(t_{PCBSYR}). While the data in the cache registers is read out in 30ns cycle time by sequentially pulsing RE, data of next page is transferred to the data registers. By issuing Last Cache Read command(3Fh), last data is transferred to the cache registers from the data registers after the completion of transfer from memory cell to data registers. Cache Read is available only within a block.

The device has a Read operation with cache registers that enables the high speed read operation shown below. When the block address changes, this sequence has to be started from the beginning.

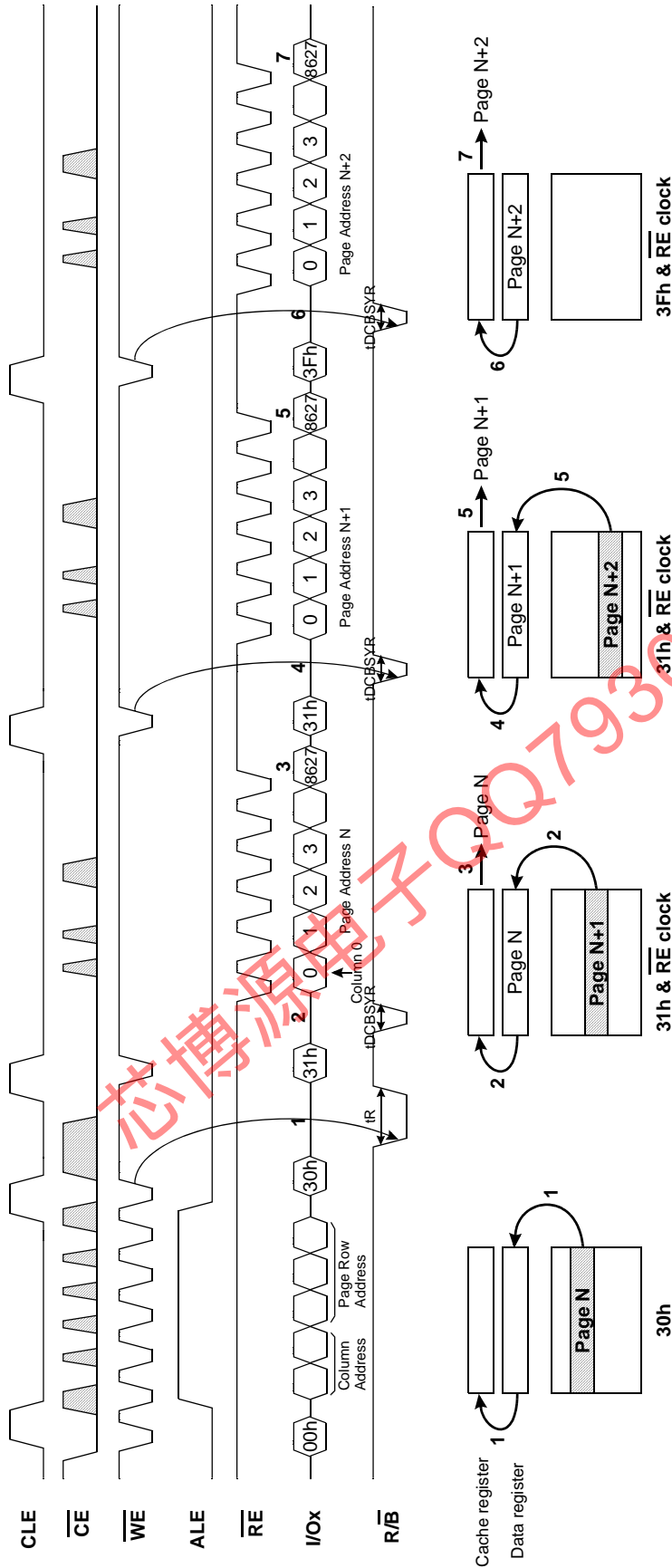


Figure 8. Cache Read

NOTE

- If the 31h command is issued to the device, the data content of the next page is transferred to the data registers during serial data out from the cache registers, and therefore the tR (Data transfer from memory cell to data register) will be reduced.
- 1. Normal read. Data is transferred from Page N to cache registers through data registers. During this time period, the device outputs Busy state for tR max.
- 2. After the Ready/Busy returns to Ready, 31h command is issued and data is transferred to cache registers from data registers again. This data transfer takes tDCBSYR max and the completion of this time period can be detected by Ready/Busy signal.
- 3. Data of Page N+1 is transferred to data registers from cell while the data of Page N in cache registers can be read out by RE clock simultaneously.
- 4. The 31h command makes data of Page N+1 transfer to cache registers from data registers after the completion of the transfer from cell to data registers. The device outputs Busy state for tDCBSYR max. This Busy period depends on the combination of the internal data transfer time from cell to data registers and the serial data out time.
- 5. Data of Page N+2 is transferred to data registers from cell while the data of Page N+1 in cache registers can be read out by RE clock simultaneously.
- 6. The 3Fh command makes the data of Page N+2 transfer to the cache registers from the data registers after the completion of transfer from cell to data registers. The device outputs Busy state for tDCBSYR max. This Busy period depends on the combination of the internal data transfer time from cell to data registers and the transfer from data registers to cache registers.
- 7. Data of Page N+2 in cache registers can be read out, but since the 3Fh command does not transfer the data from the memory cell to data registers, the device can accept new command input immediately after the completion of serial data out.

5.3 Page Program

The device is programmed basically on a page basis, and the number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 1 time for the page. The addressing should be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 8,628bytes of data may be loaded into the data registers via cache registers, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the five cycle address inputs and then serial data loading. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address for the next data, which will be entered, may be changed to the address which follows random data input command(85h). Random data input may be operated multiple times regardless of how many times it is done in a page.

The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

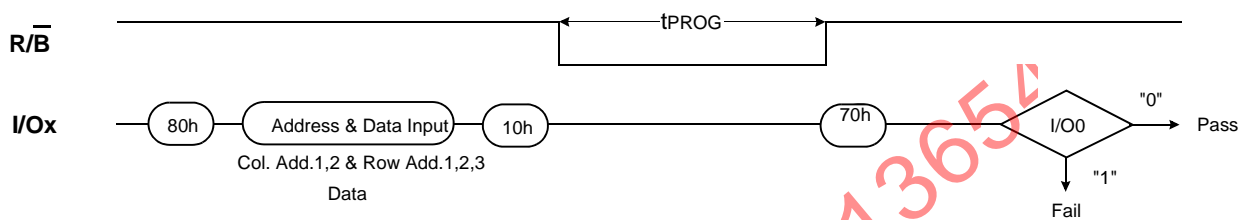


Figure 9. Program & Read Status Operation

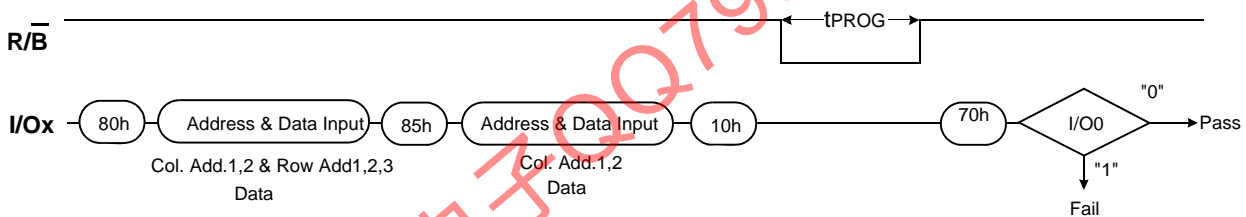


Figure 10. Random Data Input In a Page

5.4 Copy-back Program

Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in one page without data re-loading when the bit error is not in data stored. Since the time-consuming re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with "35h" command and the address of the source page moves the whole 8,628byte data into the internal data buffer. A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register. When the Copy-Back Program is complete, the Write Status Bit(I/O 0) may be checked. The command register remains in Read Status command mode until another valid command is written to the command register.

During copy-back program, data modification is possible using random data input command (85h) as shown below.

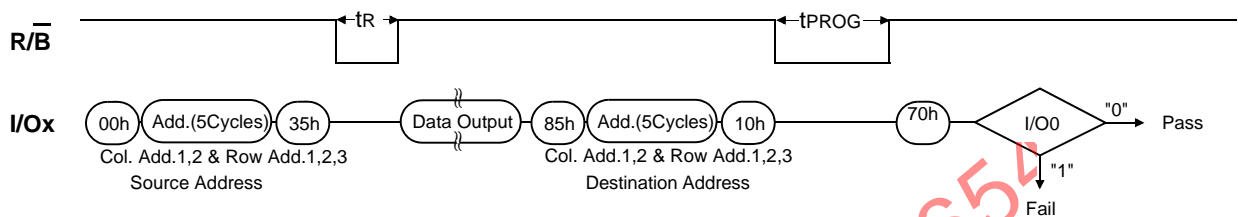


Figure 11. Page Copy-Back Program Operation

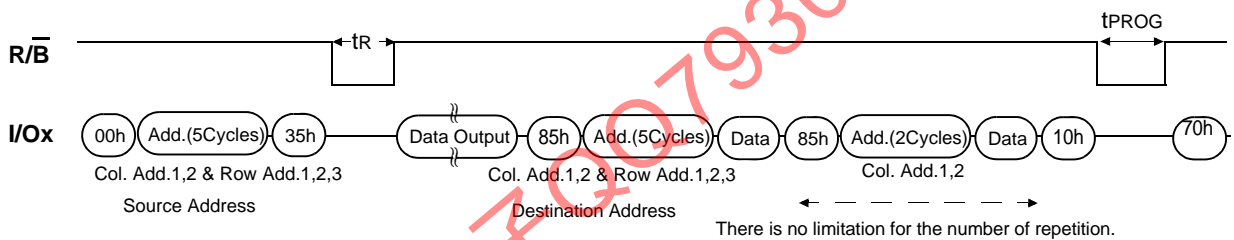


Figure 12. Page Copy-Back Program Operation with Random Data Input

5.5 Cache Program

Cache Program is an extension of Page Program, which is executed with 8,628byte data registers, and is available only within a block. Since the device has 1 page of cache memory, serial data input may be executed while data stored in data registers are programmed into memory cell.

After writing the first set of data up to 8,628byte into the selected cache registers, Cache Program command (15h) instead of actual Page Program (10h) is inputted to make cache registers free and to start internal program operation. To transfer data from cache registers to data registers, the device remains in Busy state for a short period of time(t_{CBSY}) and has its cache registers ready for the next data-input while the internal programming gets started with the data loaded into data registers. Read Status command (70h) may be issued to find out when cache registers become ready by polling the Cache-Busy status bit(I/O 6). Pass/fail status of only the previous page is available upon the return to Ready state. When the next set of data is inputted with the Cache Program command, t_{CBSY} is affected by the progress of pending internal programming. The programming of the cache registers is initiated only when the pending program cycle is finished and the data registers are available for the transfer of data from cache registers. The status bit(I/O5) for internal Ready/Busy may be polled to identify the completion of internal programming. If the system monitors the progress of programming only with R/\bar{B} , the last page of the target programming sequence must be programmed with actual Page Program command (10h).

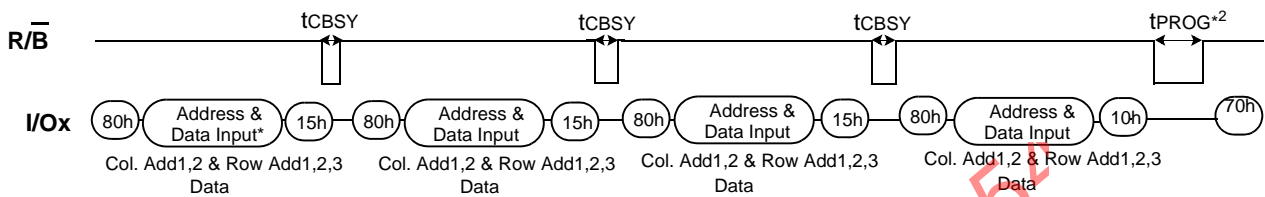


Figure 13. Cache Program(1/2)

NOTE :

1) Cache Read operation is available only within a block.

2) Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula.

$t_{PROG} = \text{Program time for the last page} + \text{Program time for the } (\text{last} - 1)^{\text{th}} \text{ page} - (\text{Program command cycle time} + \text{Last page data loading time})$

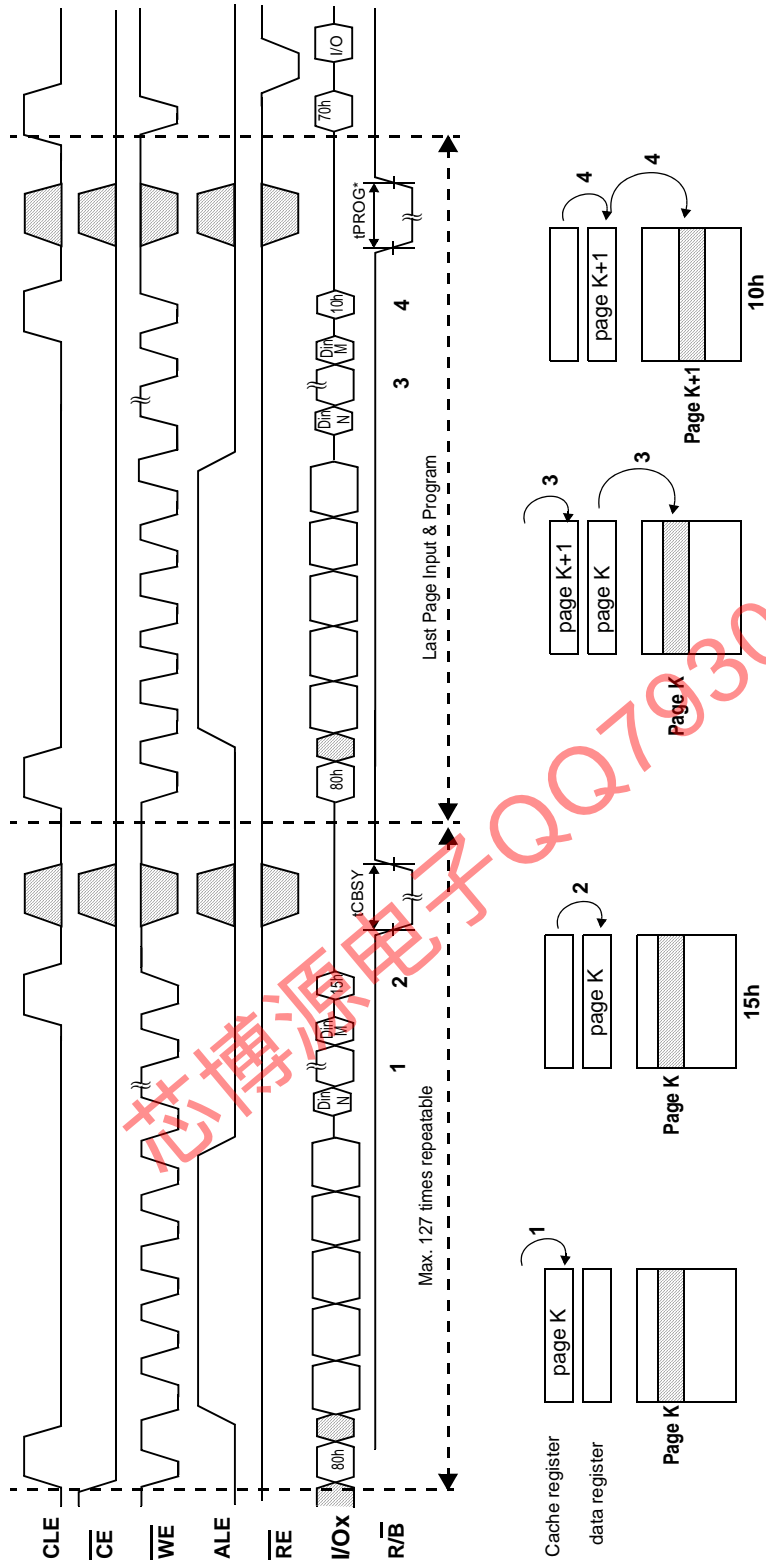


Figure 14. Cache Program(2/2)

NOTE :

- Issuing the 15h command to the device after serial data input initiates the program operation with cache registers.
- 1. Data for Page K is input to cache registers.
- 2. Data is transferred to the data registers by the 15h command. During the transfer the Ready/Busy outputs Busy State (ICBSY).
- 3. Data for Page K+1 is input to cache registers while the data of the Page K is being programmed.
- 4. The programming with cache registers is terminated by the 10h command . When the device becomes Ready, it shows that the internal programming of the Page K+1 is completed.

tPROG* = Program time for the last page + Program time for the (last -1)th page - (command input cycle time + address input cycle time + Last page data loading time)

Pass/Fail status for each page programmed by the Cache Program operation can be detected by the Read Status operation.

- I/O 0 : Pass/Fail of the current page program operation.
- I/O 1 : Pass/Fail of the previous page program operation.

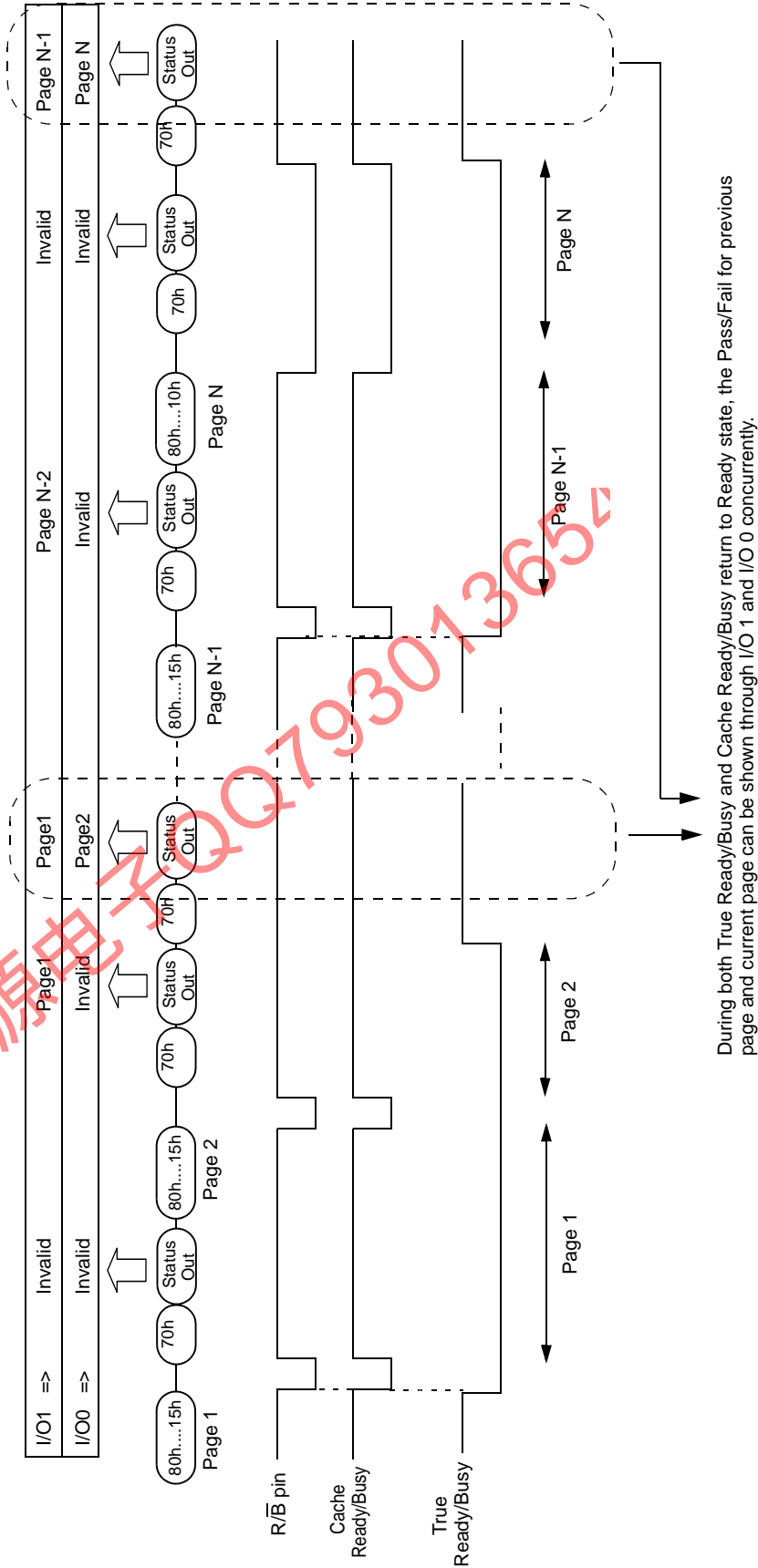
The Pass/Fail status on I/O 0 and I/O 1 are valid under the following conditions.

- Status on I/O 0 : True Ready/Busy is Ready state.
- Status on I/O 1 : Cache Read/Busy is Ready State.

The True Ready/Busy is output on I/O 5 by Read Status operation or R/B pin after the 10h command.

The Cache Ready/Busy is output on I/O 6 by Read Status operation or R/B pin after the 15h command.

Example)



5.6 Block Erase

The Erase operation is done on a block basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command(60h). Only Block address are valid while Page address is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of \overline{WE} after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 20 details the sequence.

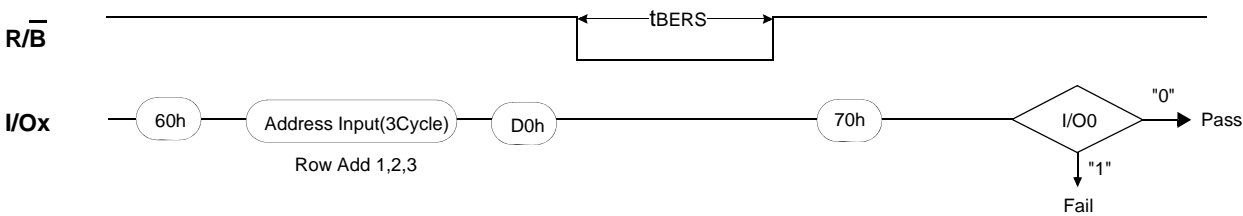


Figure 15. Block Erase Operation

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5.7 Read Status

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h or F1h/F2h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of \overline{CE} or \overline{RE} , whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired. \overline{RE} or \overline{CE} does not need to be toggled for updated status. Refer to Table 2 for specific 70h Status Register definitions and Table 3 for specific F1h status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command(00h) should be given before starting read cycles.

[Table 4] Status Register Definition for 70h Command

I/O	Page Program	Block Erase	Cache Program	Read	Cache Read	Definition
I/O 0	Pass/Fail	Pass/Fail	Pass/Fail(N)	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 1	Not Use	Not Use	Pass/Fail(N-1)	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 2	Not Use	Not Use	Not Use	Not Use	Not Use	Don't-cared
I/O 3	Not Use	Not Use	Not Use	Not Use	Not Use	Don't-cared
I/O 4	Not Use	Not Use	Not Use	Not Use	Not Use	Don't-cared
I/O 5	Not Use	Not Use	True Ready/Busy	Not Use	True Ready/Busy	Busy : "0" Ready : "1"
I/O 6	Ready/Busy	Ready/Busy	Cache Ready/Busy	Ready/Busy	Cache Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected : "0" Not Protected : "1"

NOTE :

- 1) I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.
- 2) N : current page, N-1 : previous page.

[Table 5] F1h Read Status Register Definition

I/O	Page Program	Block Erase	Cache Program	Read	Cache Read	Definition
I/O 0	Chip1 Pass/Fail	Chip1 Pass/Fail	Chip1 Pass/Fail(N)	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 1	Plane Pass/Fail	Plane Pass/Fail	Plane Pass/Fail(N)	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 2	Not Use	Not Use	Not Use	Not Use	Not Use	Don't-cared
I/O 3	Not Use	Not Use	Plane Pass/Fail(N-1)	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 4	Not Use	Not Use	Not Use	Not Use	Not Use	Don't-cared
I/O 5	Not Use	Not Use	True Ready/Busy	Not Use	True Ready/Busy	Busy : "0" Ready : "1"
I/O 6	Ready/Busy	Ready/Busy	Cache Ready/Cache	Ready/Busy	Cache Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected : "0" Not Protected : "1"

NOTE :

- 1) I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.
- 2) N : current page, N-1 : previous page.

[Table 6] F2h Read Status Register Definition

I/O	Page Program	Block Erase	Cache Program	Read	Cache Read	Definition
I/O 0	Chip2 Pass/Fail	Chip2 Pass/Fail	Chip2 Pass/Fail(N)	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 1	Plane Pass/Fail	Plane Pass/Fail	Plane Pass/Fail(N)	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 2	Not Use	Not Use	Not Use	Not Use	Not Use	Don't-cared
I/O 3	Not Use	Not Use	Plane Pass/Fail(N-1)	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 4	Not Use	Not Use	Not Use	Not Use	Not Use	Don't-cared
I/O 5	Not Use	Not Use	True Ready/Busy	Not Use	True Ready/Busy	Busy : "0" Ready : "1"
I/O 6	Ready/Busy	Ready/Busy	Cache Ready/Cache	Ready/Busy	Cache Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected : "0" Not Protected : "1"

NOTE :

- 1) I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.
- 2) N : current page, N-1 : previous page.

5.8 Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Six read cycles sequentially output the manufacturer code(ECh), the device code, 3rd, 4th, 5th and 6th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 22 shows the operation sequence.

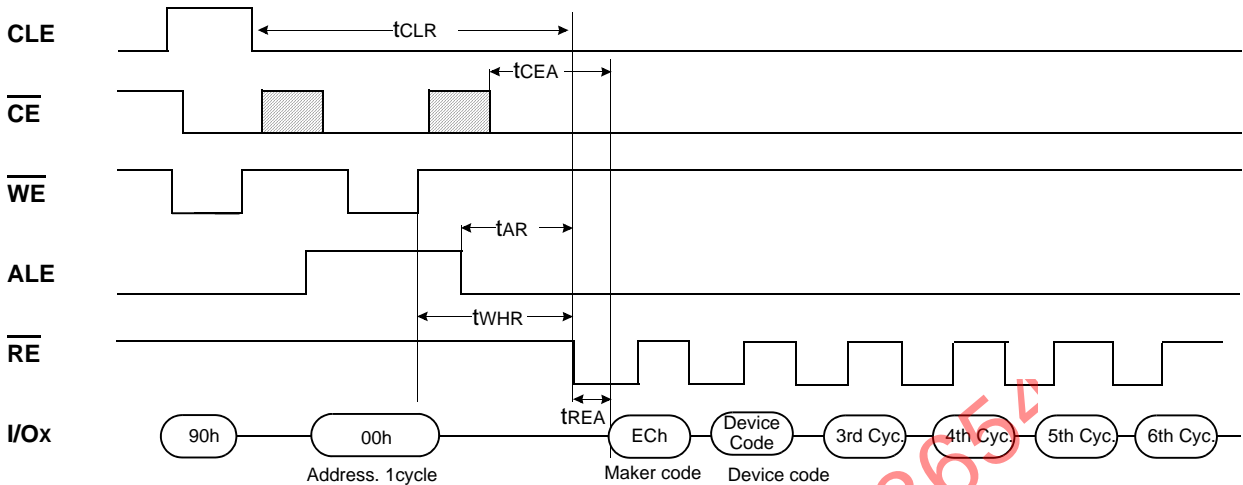


Figure 16. Read ID Operation

Device	Device Code (2nd Cycle)	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
K9GAG08U0E	D5h	84h	72h	50h	42h
K9LBG08U0E	D7h	C5h		54h	
K9HCG08U1E					

5.9 RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP is high. Refer to Table 7 for device status after reset operation. If the device is already in reset state a new reset command will be accepted by the command register. The R/B pin changes to low for tRST after the Reset command is written. Refer to Figure 17 below.



Figure 17. RESET Operation

[Table 7] Device Status

	After Reset
Operation Mode	Waiting for next command

5.10 Ready/ $\overline{\text{Busy}}$

The device has a $\overline{\text{R/B}}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The $\overline{\text{R/B}}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more $\overline{\text{R/B}}$ outputs to be Or-tied. Because pull-up resistor value is related to $t_r(\overline{\text{R/B}})$ and current drain during busy(i_{busy}), an appropriate value can be obtained with the following reference chart(Figure 18). Its value can be determined by the following guidance.

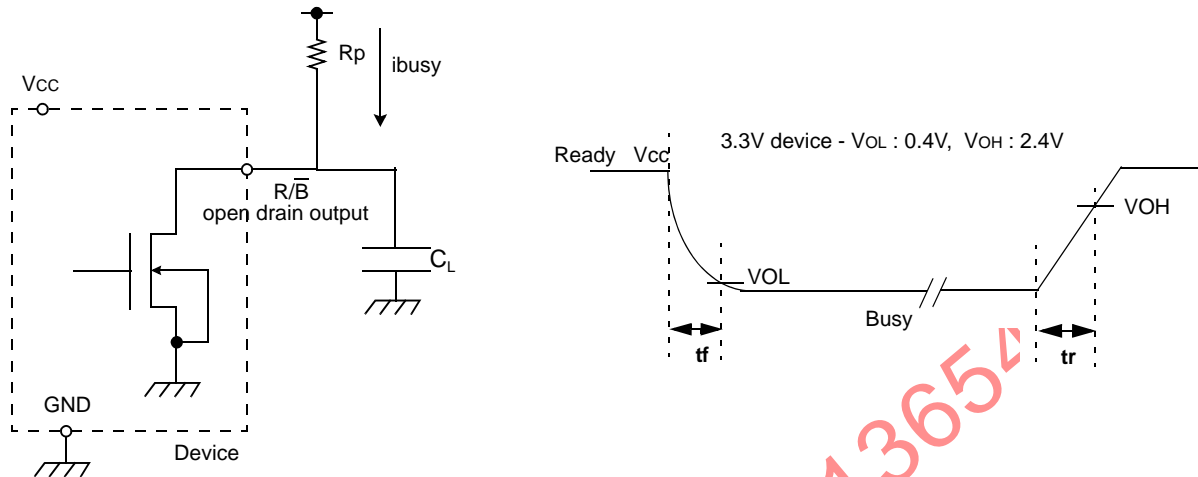
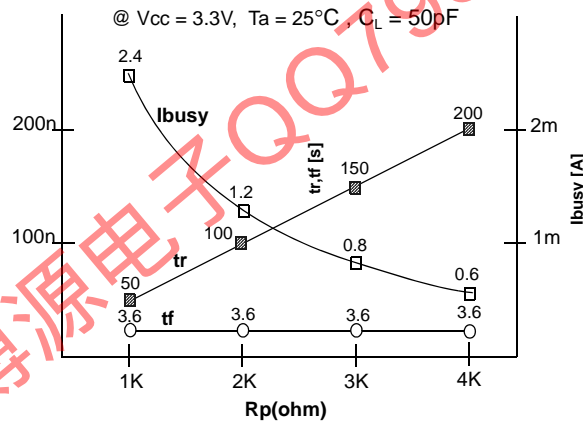


Figure 18. R_p vs t_r , t_f & R_p vs i_{busy}



R_p value guidance

$$R_p(\text{min, 3.3V part}) = \frac{V_{\text{cc}}(\text{Max.}) - V_{\text{OL}}(\text{Max.})}{I_{\text{OL}} + \sum I_L} = \frac{3.2\text{V}}{8\text{mA} + \sum I_L}$$

where I_L is the sum of the input currents of all devices tied to the $\overline{\text{R/B}}$ pin.

$R_p(\text{max})$ is determined by maximum permissible limit of t_r

6.0 DATA PROTECTION & POWER UP SEQUENCE

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2V. The Reset command(FH) must be issued to all CEs as the first command after the NAND Flash device is powered on. Each CE will be busy for a maximum of 5ms after a RESET command is issued. In this time period, the acceptable command is 70h/F1h/F2h. WP pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. The two step command sequence for program/erase provides additional software protection.

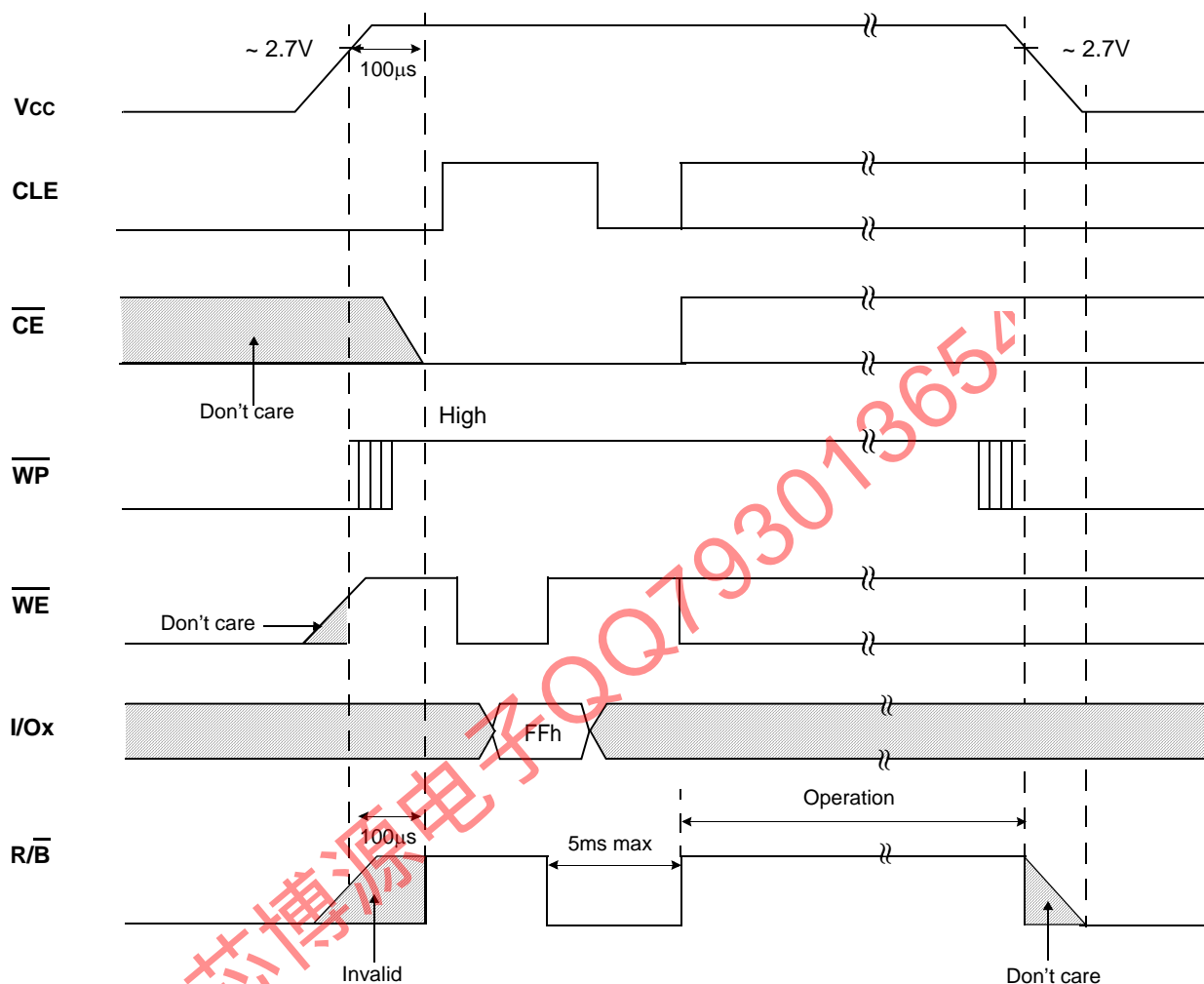


Figure 19. AC Waveforms for Power Transition

NOTE :
During the initialization, the device consumes a maximum current of 50mA (ICC1)

6.1 WP AC Timing guide

Enabling WP during erase and program busy is prohibited. The erase and program operations are enabled and disabled as follows:

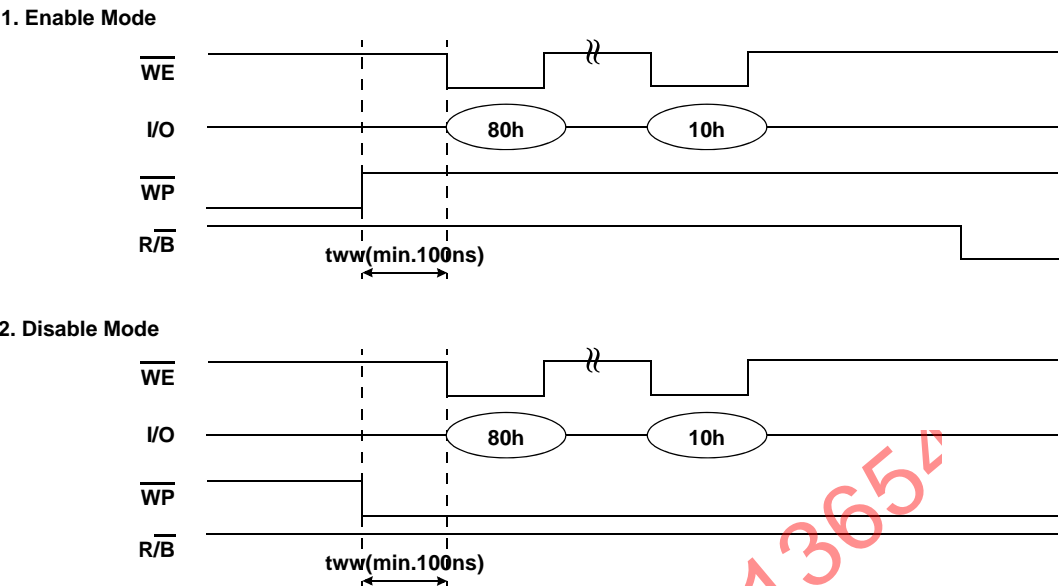


Figure B-1. Program Operation

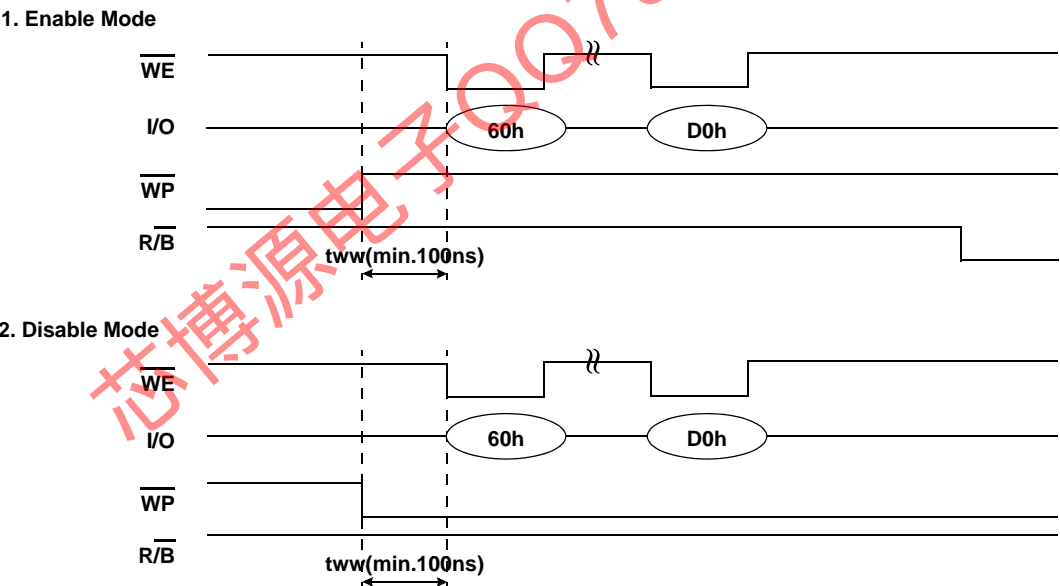


Figure B-2. Erase Operation