First Semiconductor

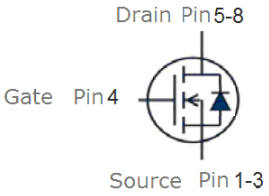
FIR30N03D3G

30V/30A N-Channel Advanced Power MOSFET-C

PIN Connection DFN3*3

Features:

- High ruggedness
- Enhancement mode
- Very low on-resistance $R_{DS(on)}$ Typ8.7mΩ@ V_{GS}=4.5 V
  Typ5.7mΩ@ VGS=10 V
- Low Gate Charge Typ 34nC
- 100% Avalanche test
- Improved dv/dt Capability
- Application:Synchronous
  Rectification Li Battery Protect Board, Inverter



Marking Diagram

Y = Year
A = Assembly Location
WW = Work Week
FIR30N03D3 = Specific Device Code

Absolute Maximum Ratings* (Tc=25℃ Unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	30	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	27	A
Pulsed Drain Current (Note 1)	I_{DM}	232	A
Maximum Power Dissipation	P_D	30	W
Single pulse avalanche energy (Note 5)	E_{AS}	72	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristics

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JC}$	4.1	℃/W
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	61	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	30		-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.2	1.6	2.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=15A	-	5.7	6.6	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V, I_D=15A	-	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=15V,V_{GS}=0V, F=1.0MHz	-	1507	-	PF
Output Capacitance	C_{oss}		-	198	-	PF
Reverse Transfer Capacitance	C_{rss}		-	196	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=15V,I_D=15A, V_{GS}=10V,R_G=6Ω	-	5	-	nS
Turn-on Rise Time	t_r		-	25	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	19	-	nS
Turn-Off Fall Time	t_f		-	12	-	nS
Total Gate Charge	Q_g	V_{DS}=15V,I_D=15A , V_{GS}=10V	-	34		nC
Gate-Source Charge	Q_{gs}		-	5	-	nC
Gate-Drain Charge	Q_{gd}		-	11	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=15A	-	-	1.4	V
Reverse Recovery Time	t_{rr}		-	6.3	-	nS
Reverse Recovery Charge	Q_{rr}		-	1.3	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. Limited by TJmax, starting TJ = 25°C, L = 0.5mH, RG = 25Ω, IAS = 10A, VGS =10V. Part not recommended for use above this value .

Fig. 1. On-state characteristics

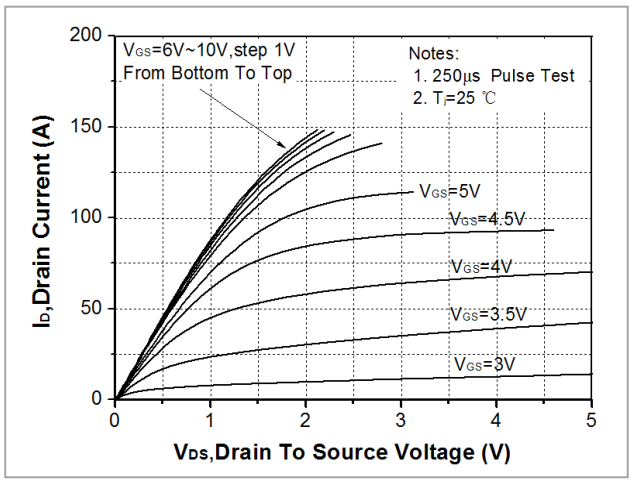


Fig. 2. Transfer Characteristics

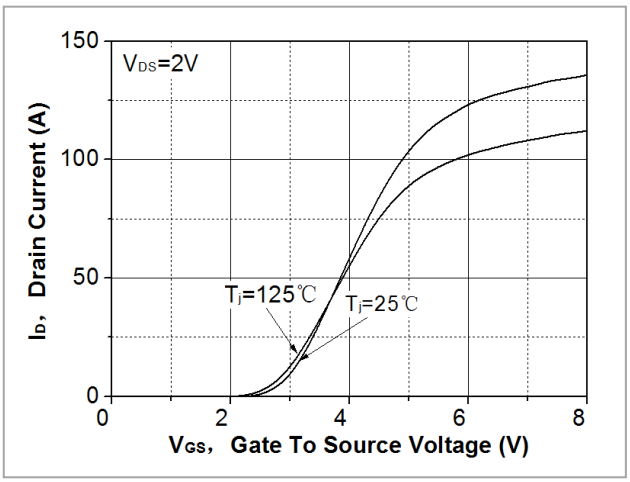


Fig. 3. On-resistance variation vs. drain current and gate voltage

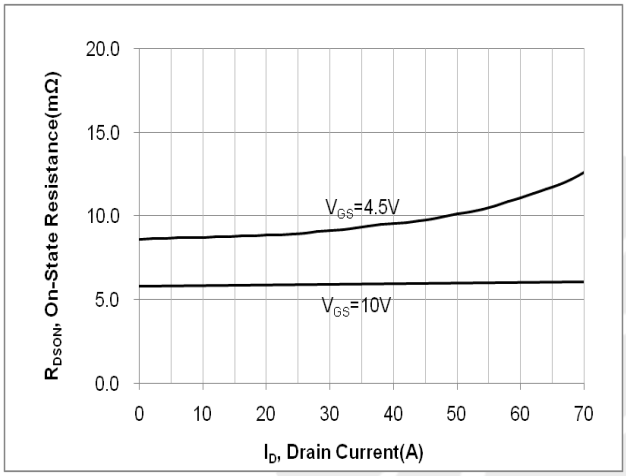


Fig. 4. On-state current vs. diode forward voltage

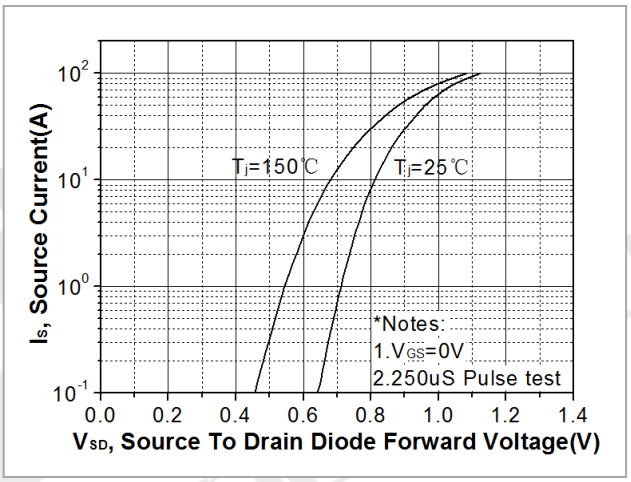


Fig 5. Breakdown voltage variation vs. junction temperature

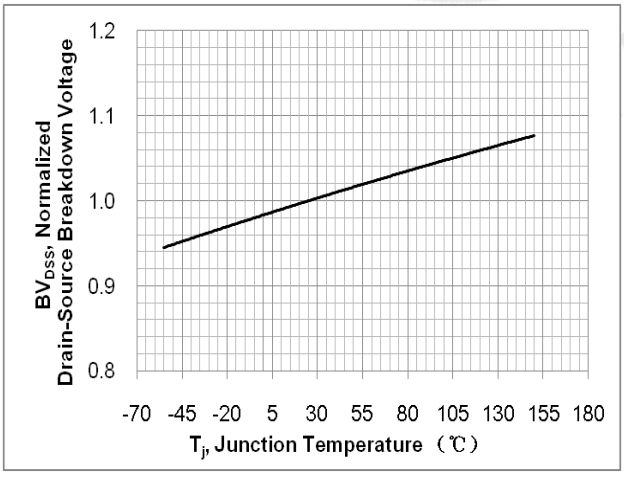


Fig. 6. On-resistance variation vs. junction temperature

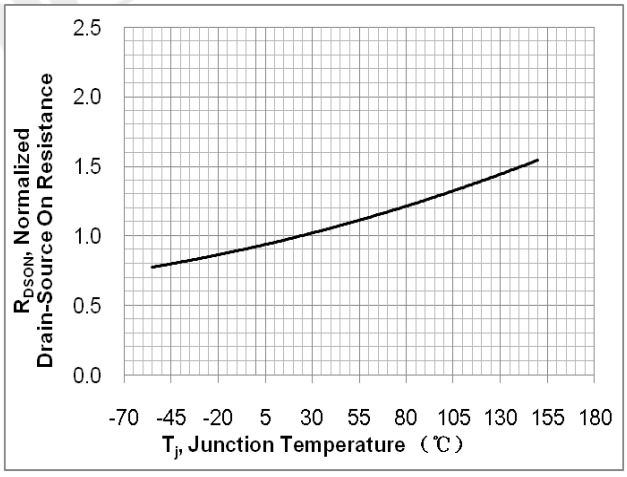


Fig. 7. Gate charge characteristics

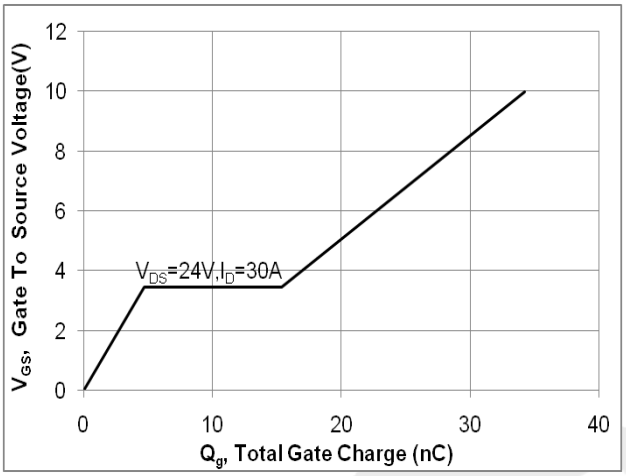


Fig. 8. Capacitance Characteristics

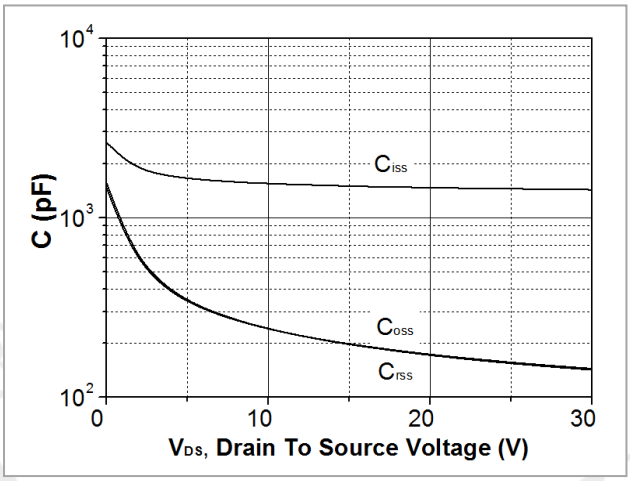


Fig. 9. Maximum safe operating area

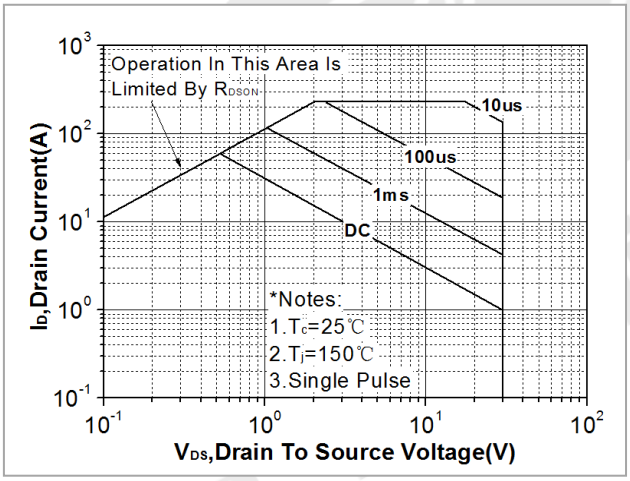


Fig. 10. Maximum drain current vs. case temperature

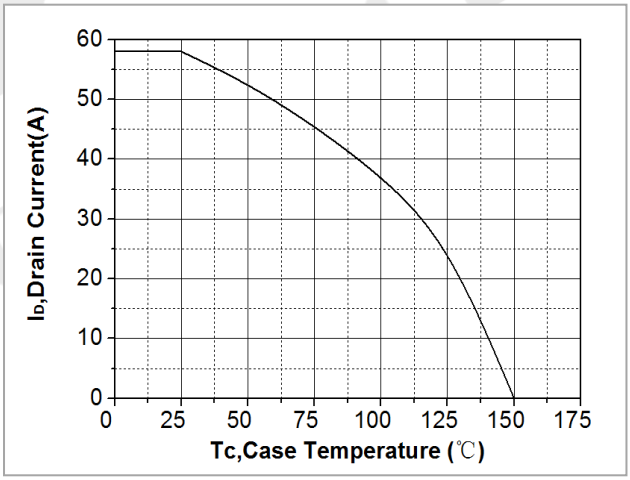


Fig. 11. Transient thermal response curve

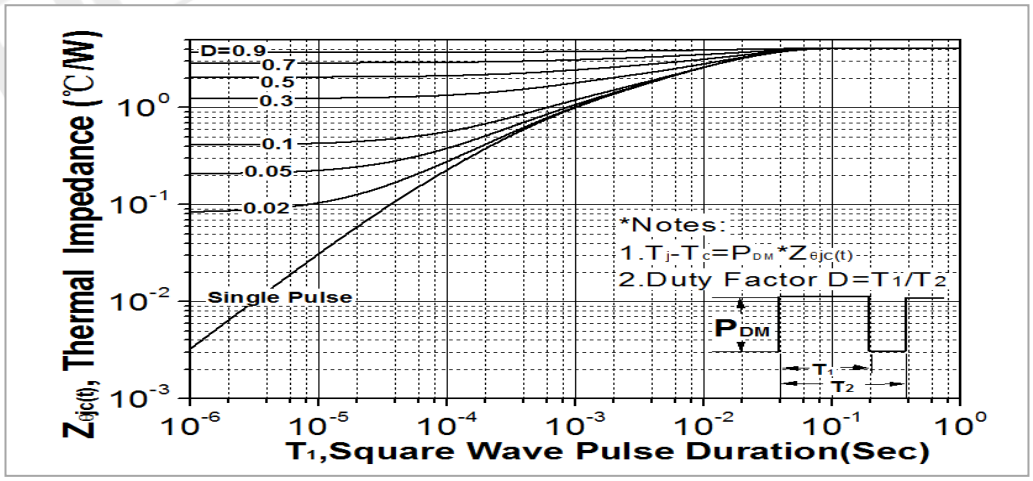


Fig. 12. Gate charge test circuit & waveform

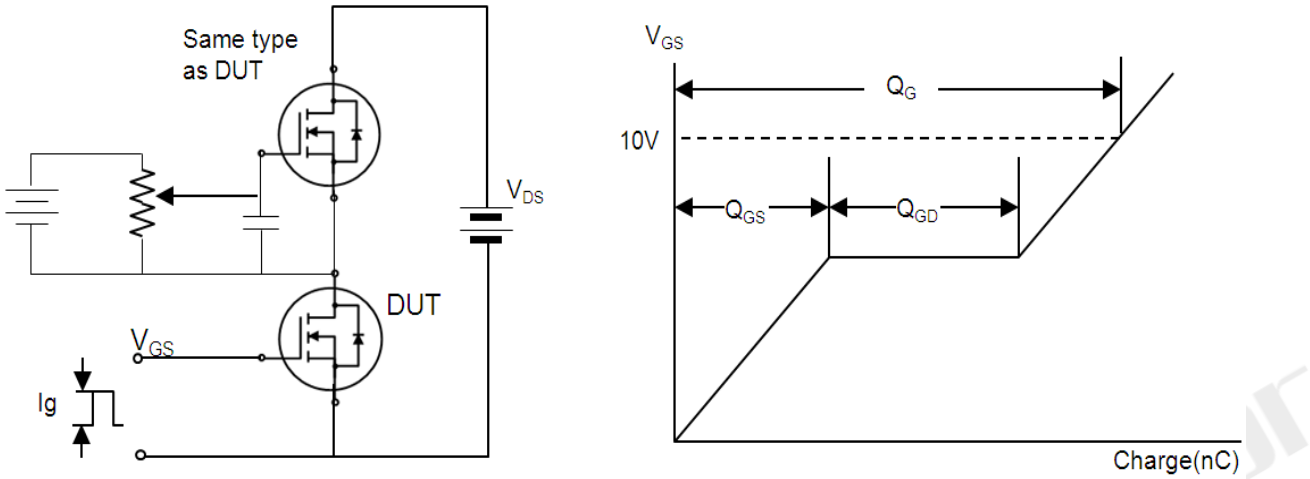


Fig. 13. Switching time test circuit & waveform

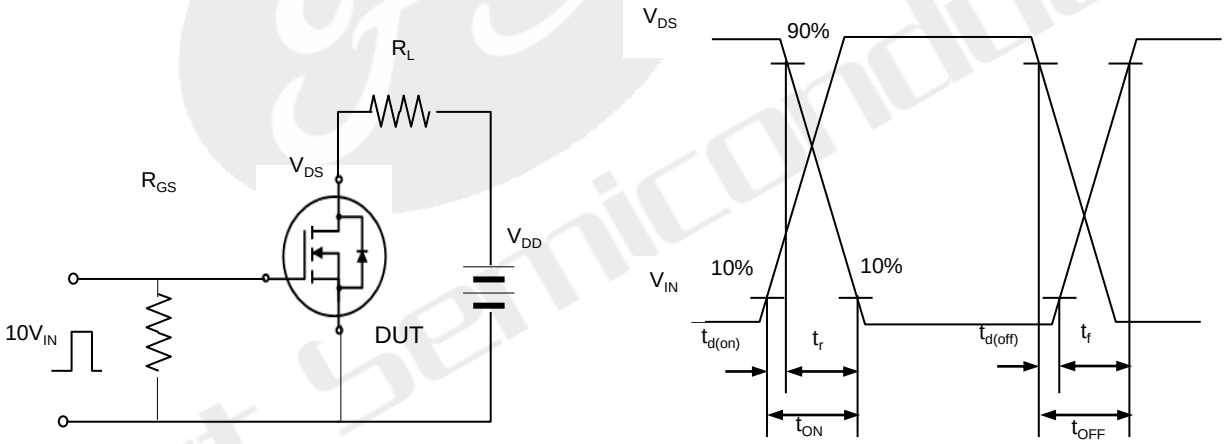


Fig. 14. Unclamped Inductive switching test circuit & waveform

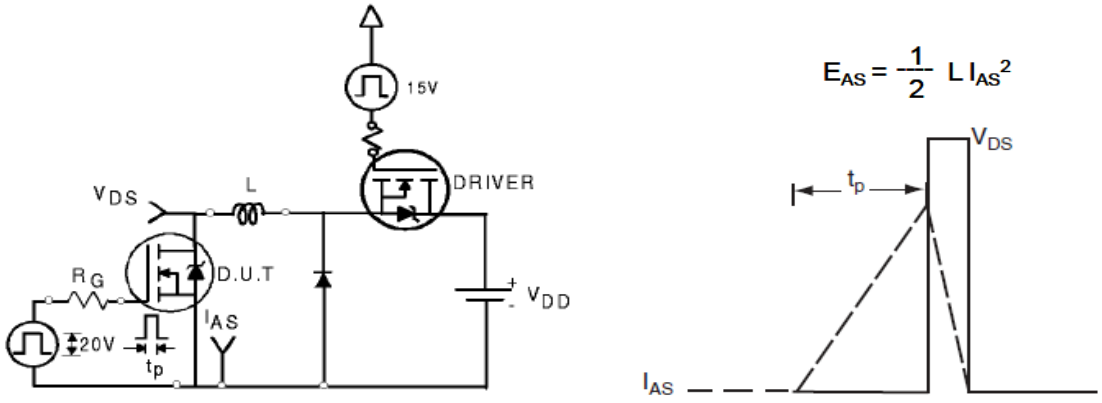
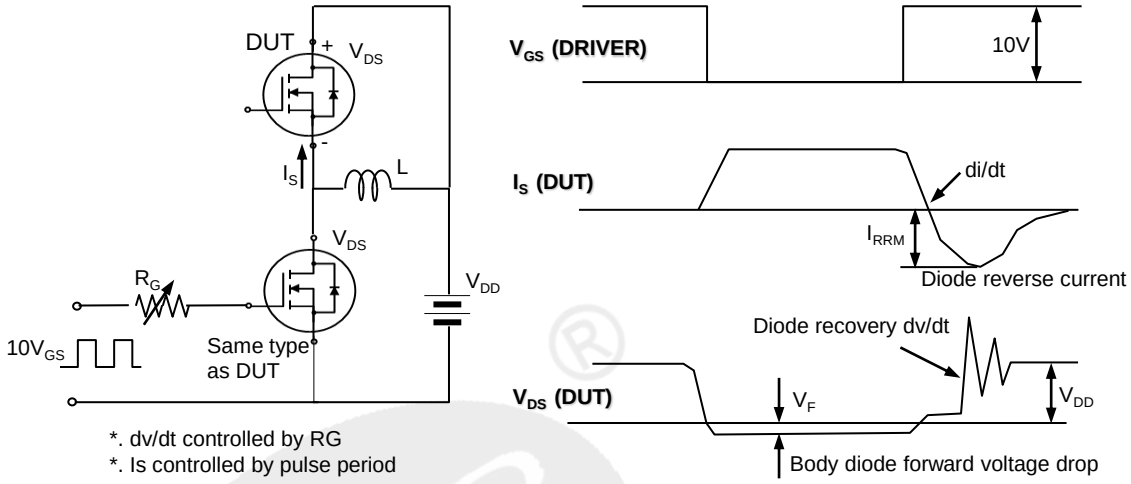
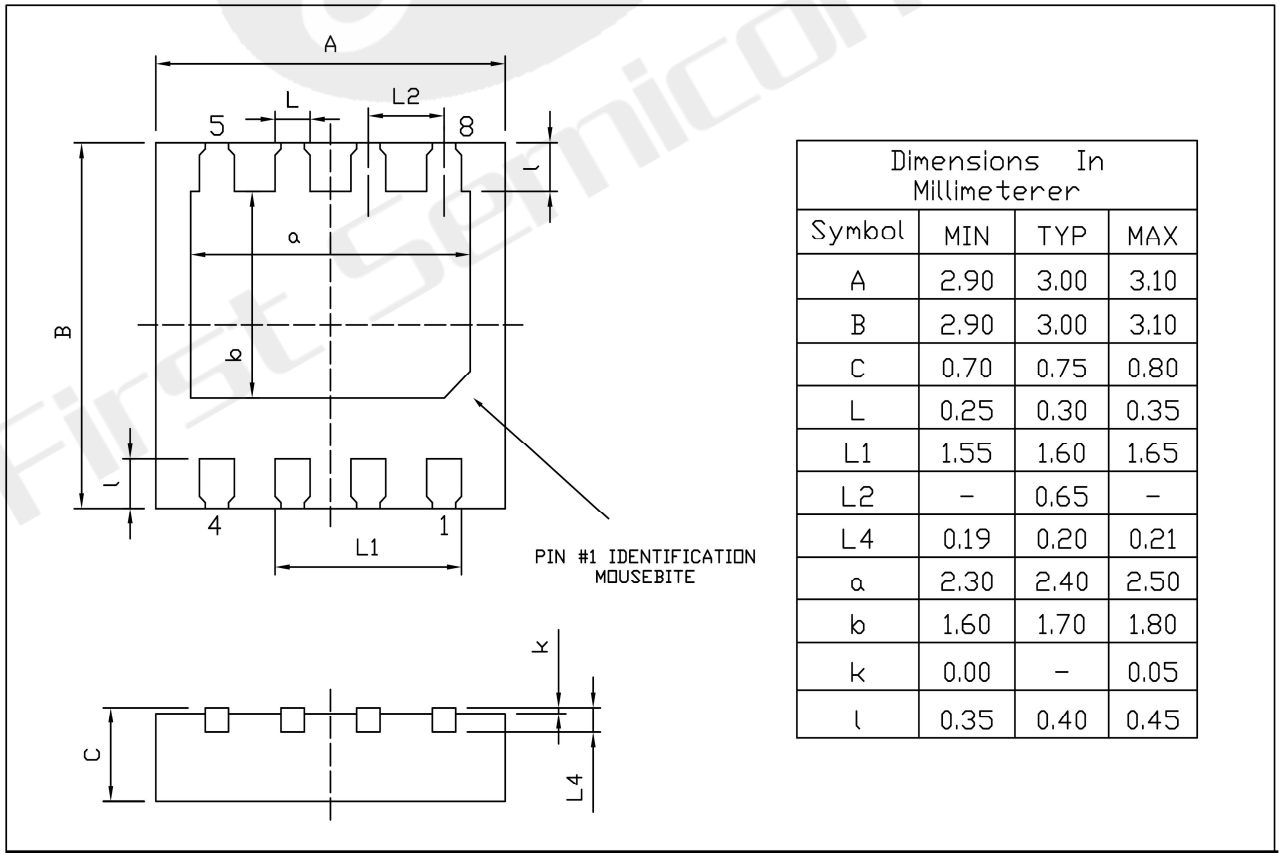


Fig. 15. Peak diode recovery dv/dt test circuit & waveform



Package Information

DFN3X3A-8L Unit:mm



Dimensions In Millimeterer			
Symbol	MIN	TYP	MAX
A	2.90	3.00	3.10
B	2.90	3.00	3.10
C	0.70	0.75	0.80
L	0.25	0.30	0.35
L1	1.55	1.60	1.65
L2	-	0.65	-
L4	0.19	0.20	0.21
a	2.30	2.40	2.50
b	1.60	1.70	1.80
k	0.00	-	0.05
l	0.35	0.40	0.45

Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure,The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing,To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2022.06.01	1.0	Initial release	