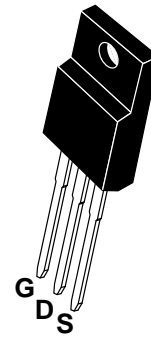
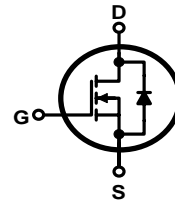




PIN Connection TO-220F



Schematic diagram



Marking Diagram



- Y = Year
- A = Assembly Location
- WW = Work Week
- VT = Version & Thickness
- FIR7N65F = Specific Device Code

General Description

FIR7N65FG , the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-220F, which accords with the RoHS standard.

Features

- I Fast Switching
- I Low ON Resistance
- I Low Gate Charge
- I Low Reverse transfer capacitances
- I 100% Single Pulse avalanche energy Test

Absolute Maximum Ratings (Ta = 25°C unless otherwise noted; reference only)

Characteristics	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	± 30	V
Drain Current	I_D	$T_C=25^\circ C$	7.0
		$T_C=100^\circ C$	4.4
Drain Current Pulsed	I_{DM}	28	A
Power Dissipation($T_C=25^\circ C$) -Derate above 25°C	P_D	35	W
		0.28	W/°C
Single Pulsed Avalanche Energy(Note 1)	E_{AS}	375	mJ
Operation Junction Temperature Range	T_J	-55~+150	°C
Storage Temperature Range	T_{stg}	-55~+150	°C

**Thermal Characteristics**

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.57	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	120	$^{\circ}\text{C}/\text{W}$

Electrical Characteristics (Ta = 25°C unless otherwise noted; reference only)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	25 °C, $V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	650	--	--	V
		125 °C, $V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	25 °C, $V_{DS}=650\text{V}$, $V_{GS}=0\text{V}$	--	--	1	μA
		125 °C, $V_{DS}=520\text{V}$, $V_{GS}=0\text{V}$	--	--	100	μA
		150 °C, $V_{DS}=520\text{V}$, $V_{GS}=0\text{V}$	--	--	100	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 30\text{V}$, $V_{DS}=0\text{V}$	--	--	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}$, $I_D=250\mu\text{A}$	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}$, $I_D=2\text{A}$	--	1.2	1.4	Ω
Input Capacitance	C_{iss}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHZ}$	--	1000	--	pF
Output Capacitance	C_{oss}		--	89	--	
Reverse Transfer Capacitance	C_{rss}		--	3.8	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=325\text{V}$, $I_D=4.0\text{A}$, $R_G=10\Omega$ (Note 2,3)	--	18	--	ns
Turn-on Rise Time	t_r		--	20	--	
Turn-off Delay Time	$t_{d(off)}$		--	42	--	
Turn-off Fall Time	t_f		--	19	--	
Total Gate Charge	Q_g	$V_{DS}=520\text{V}$, $I_D=4.0\text{A}$, $V_{GS}=10\text{V}$ (Note 2,3)	--	24	--	nC
Gate-Source Charge	Q_{gs}		--	5.1	--	
Gate-Drain Charge	Q_{gd}		--	9.5	--	

Source-Drain Diode Ratings And Characteristics

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	7.0	A
Pulsed Source Current	I_{SM}		--	--	28	
Diode Forward Voltage	V_{SD}	$I_S=4.0\text{A}$, $V_{GS}=0\text{V}$	--	--	1.5	V
Reverse Recovery Time	T_{rr}	$I_S=4.0\text{A}$, $V_{GS}=0\text{V}$, $dI_F/dt=100\text{A}/\mu\text{s}$	--	380	--	ns
Reverse Recovery Charge	Q_{rr}		--	1900	--	nC

Notes:

- $L=30\text{mH}$, $I_{AS}=5\text{A}$, $V_{DD}=800\text{V}$, $R_G=25\Omega$, starting $T_J=25^{\circ}\text{C}$;
- Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$;
- Essentially independent of operating temperature.

Characteristics Curve:

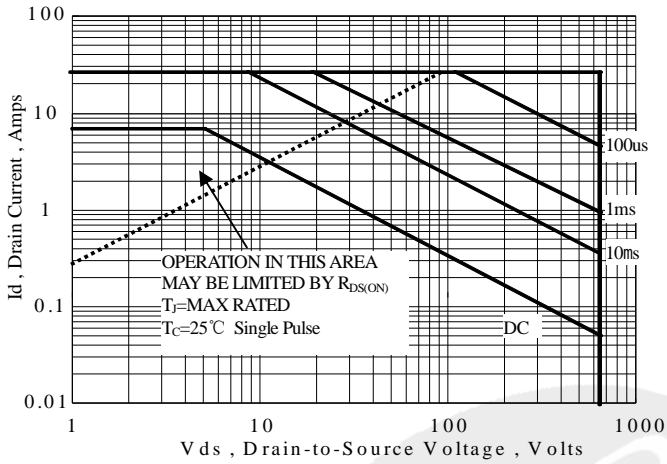


Figure 1 Maximum Forward Bias Safe Operating Area

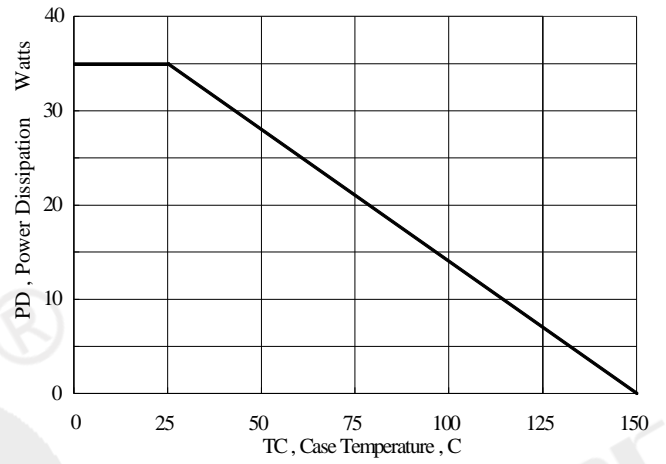


Figure 2 Maximum Power Dissipation vs Case Temperature

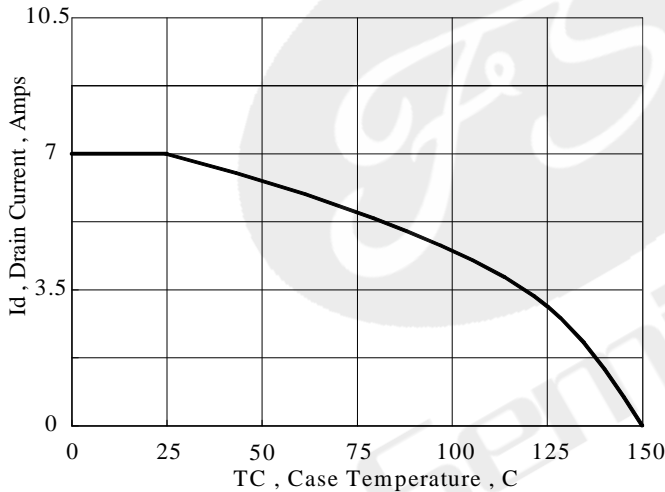


Figure 3 Maximum Continuous Drain Current vs Case Temperature

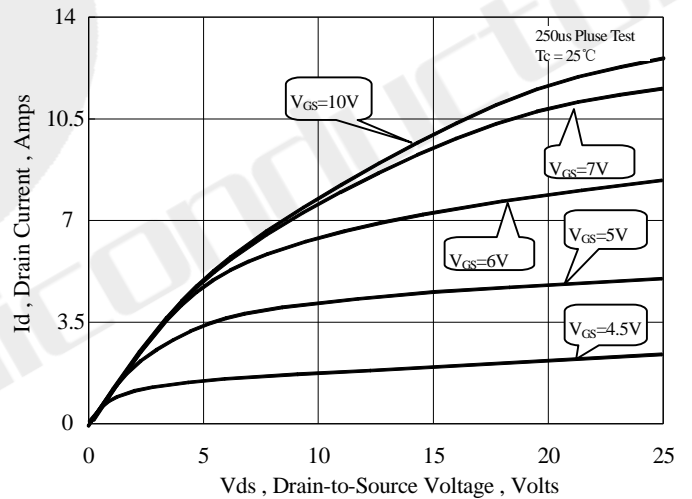


Figure 4 Typical Output Characteristics

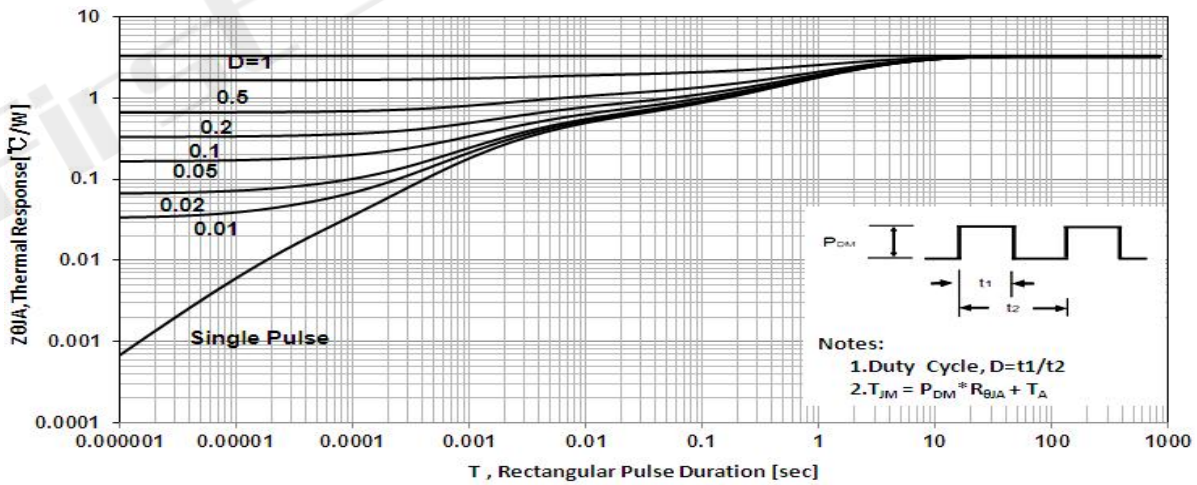


Figure 5 Maximum Effective Thermal Impedance function to Case

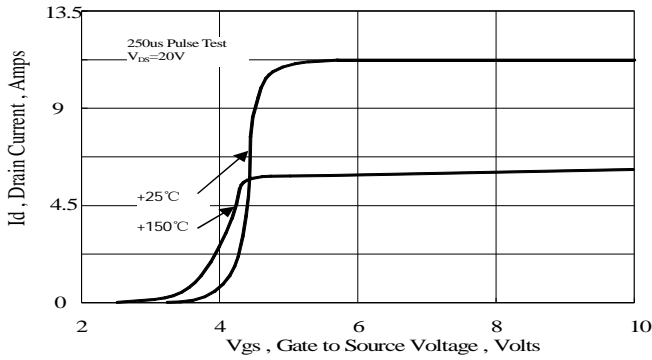


Figure 6 Typical Transfer Characteristics

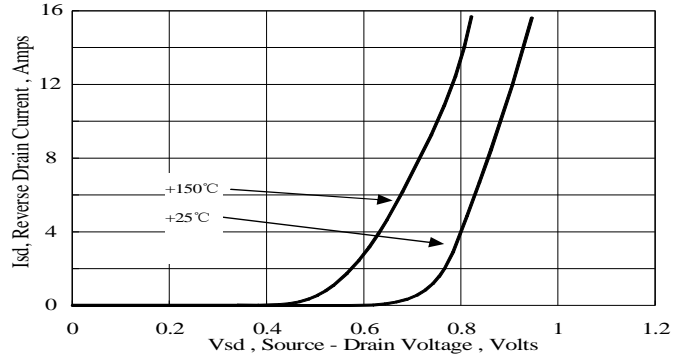


Figure 7 Typical Body Diode Transfer Characteristics

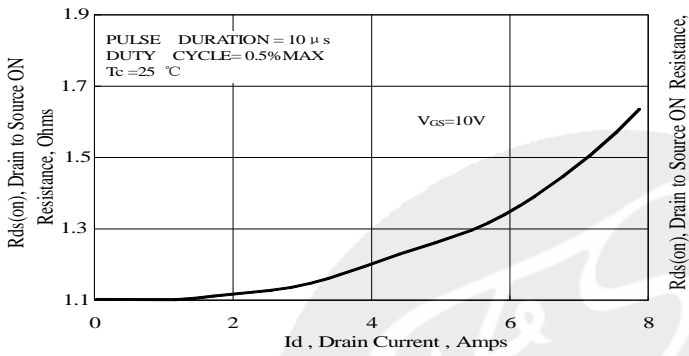


Figure 8 Typical Drain to Source ON Resistance vs Drain Current

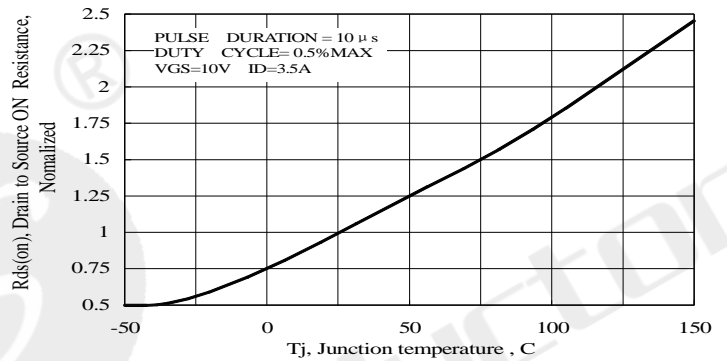


Figure 9 Typical Drain to Source on Resistance vs Junction Temperature

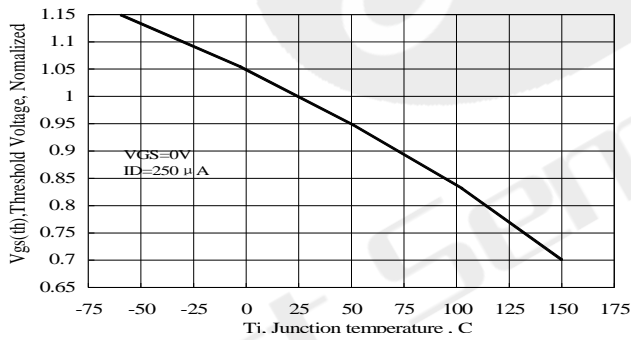


Figure 10 Typical Threshold Voltage vs Junction Temperature

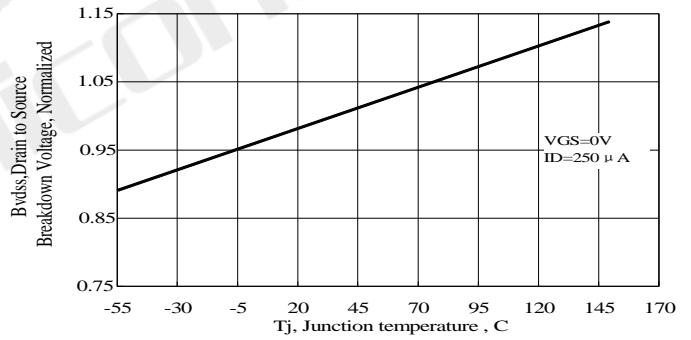


Figure 11 Typical Breakdown Voltage vs Junction Temperature

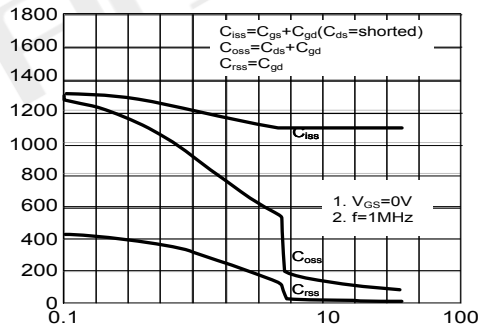


Figure 12 Typical Capacitance vs Drain to Source Voltage

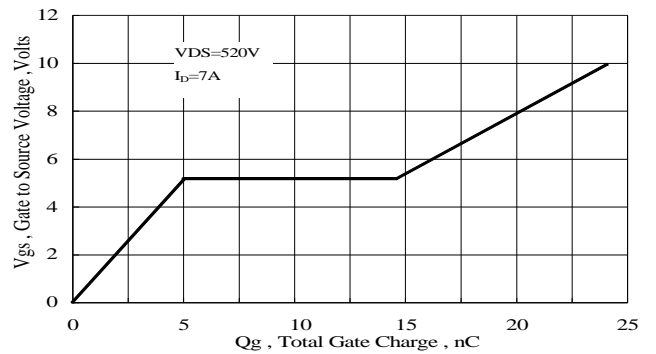


Figure 13 Typical Gate Charge vs Gate to Source Voltage

Test Circuit and Waveform

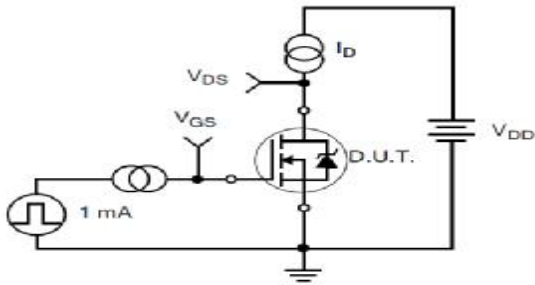


Figure 17. Gate Charge Test Circuit

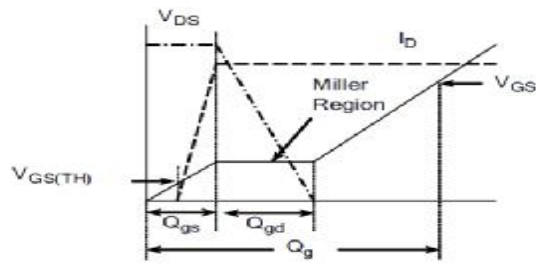


Figure 18. Gate Charge Waveform

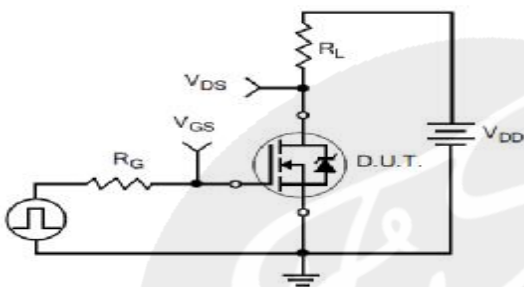


Figure 19. Resistive Switching Test Circuit

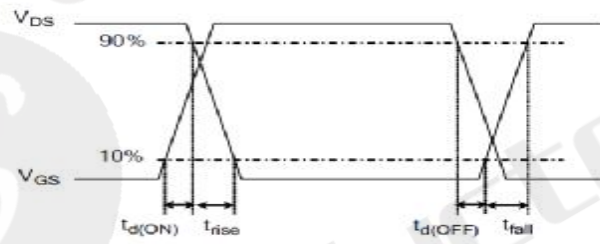


Figure 20. Resistive Switching Waveforms

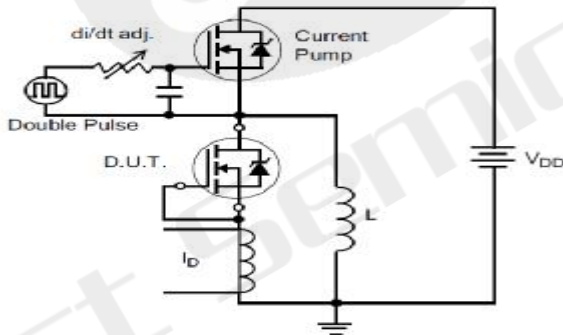


Figure 21. Diode Reverse Recovery Test Circuit

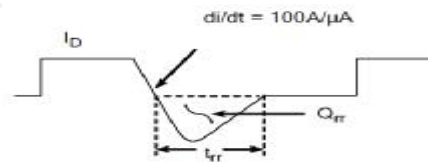


Figure 22. Diode Reverse Recovery Waveform

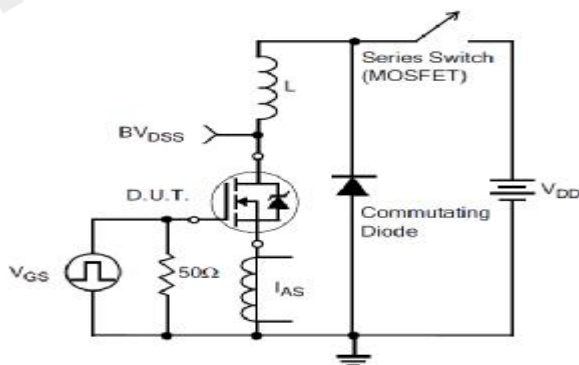


Figure 23. Unclamped Inductive Switching Test Circuit

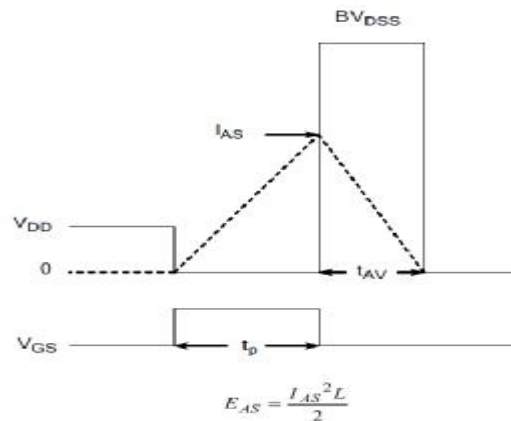


Figure 24. Unclamped Inductive Switching Waveforms



Declaration

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- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	