

20V N-Channel Enhancement Mode MOSFET

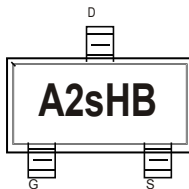
$V_{(BR)DSS}$	$R_{DS(on) Typ}$	$I_D Max$
20V	28mΩ @ 4.5V	3.0A
	32mΩ @ 3.3V	

Features

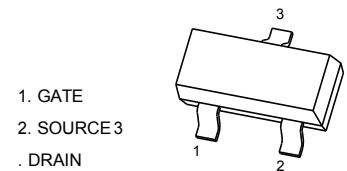
Advanced trench process technology

High Density Cell Design For Ultra Low On-Resistance

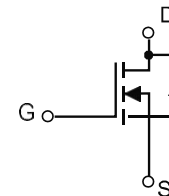
MARKING



SOT-23



Equivalent circuit



PACKAGE SPECIFICATIONS

Package	Reel Size	Reel DIA. (mm)	Q'TY/Reel (pcs)	Box Size (mm)	QTY/Box (pcs)	Carton Size (mm)	Q'TY/Carton (pcs)
SOT-23	7'	178	3000	203×203×195	45000	438×438×220	180000

Maximum Ratings (TA = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±10	
Continuous Drain Current	$T_A = 25^\circ C$	3.0	A
	$T_A = 70^\circ C$	2.5	
Pulsed Drain Current ¹⁾	I_{DM}	12	A
Maximum Power Dissipation ^{1), 2)}	$T_A = 25^\circ C$	1.2	W
	$T_A = 70^\circ C$	0.9	
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	-50 to 150	°C
Thermal Resistance from Junction-to-Ambient (t≤5s)	$R_{\theta JA}$	100	°C/W

Notes

¹⁾ Pulse width limited by maximum junction temperature.

²⁾ Surface Mounted on FR4 Board, t ≤ 5 sec.

The above data are for reference only.

MOSFET ELECTRICAL CHARACTERISTICS

$T_a=25\text{ }^{\circ}\text{C}$ unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Static						
Drain-source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D =250μA	20			V
Gate-body leakage	I _{GSS}	V _{GS} =±10V, V _{DS} =0V			±100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} =20V, V _{GS} =0V			1	μA
		V _{DS} =16V, V _{GS} =0V			100	μA
Gate-threshold voltage (note 1)	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.4	0.6	1.0	V
Drain-source on-resistance (note 1)	R _{DS(on)}	V _{GS} =4.5V, I _D =3A		28	35	mΩ
		V _{GS} =3.3V, I _D =2A		32	40	
Forward transconductance (note 1)	g _{FS}	V _{DS} =5V, I _D =3.6A		8		S
Dynamic characteristics (note 2)						
Total Gate C harge	Q _g	V _{DS} =10V, I _D =3A, V _{GS} =5V		4.7		nC
Gate-Source Charge	Q _{gs}			0.6		
Gate-Drain Charge	Q _{gd}			1.7		
Input capacitance	C _{iss}	V _{DS} =10V, V _{GS} =0V, f=1MHz		280		pF
Output capacitance	C _{oss}			46		
Reverse transfer capacitance	C _{rss}			42		
Switching characteristics						
Turn-on delay time (note 2)	t _{d(on)}	V _{DD} =10V, V _{GS} =4.5V, I _D =4A, R _G =3.3Ω		11		ns
Rise time (note 2)	t _r			35		
Turn-off delay time (note 2)	t _{d(off)}			25		
Fall time (note 2)	t _f			32		
Drain-source body diode characteristics						
Source drain current(Body Diode)	I _{SD}				1.8	A
Body diode forward voltage (note 1)	V _{SD}	I _{SD} =2A, V _{GS} = 0V		0.74	1.2	V

Notes :

- Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
- These parameters have no way to verify.

Typical Characteristics

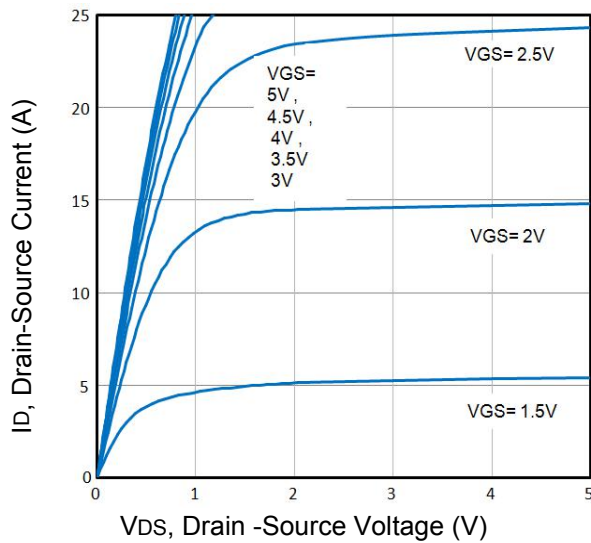


Fig1. Typical Output Characteristics

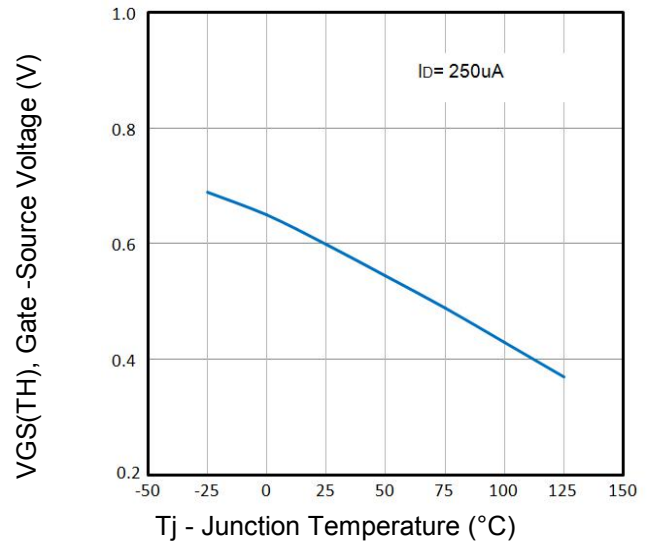


Fig2. Normalized Threshold Voltage Vs. Temperature

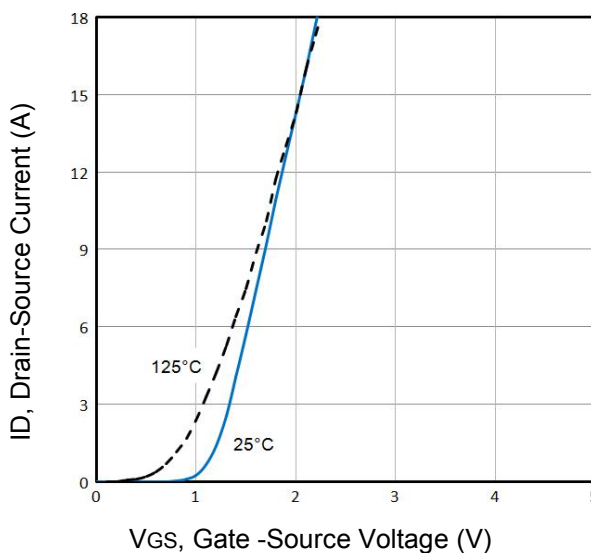


Fig3. Typical Transfer Characteristics

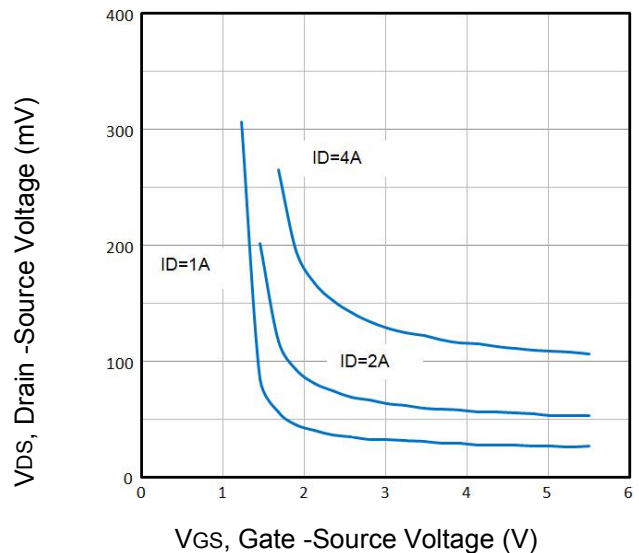
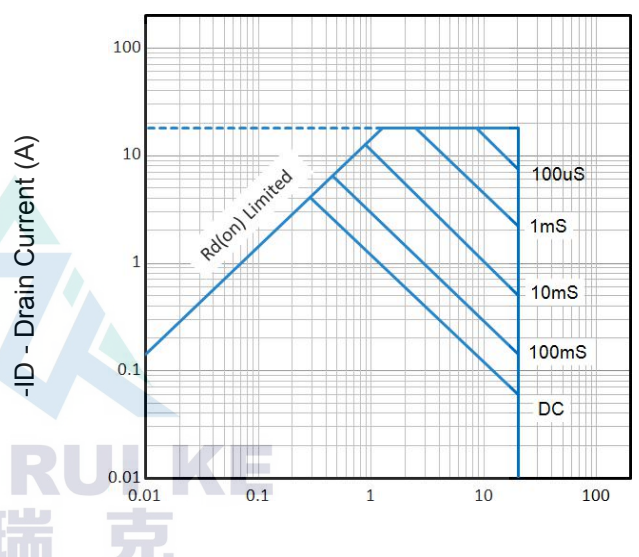
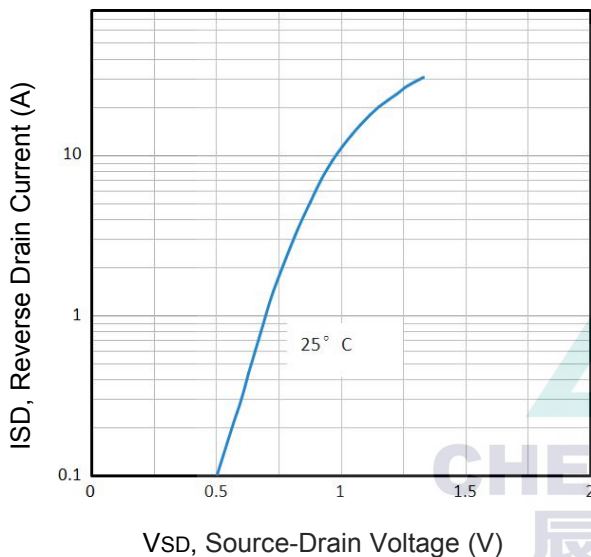


Fig4. Drain-Source Voltage vs Gate-Source Voltage



Typical Characteristics

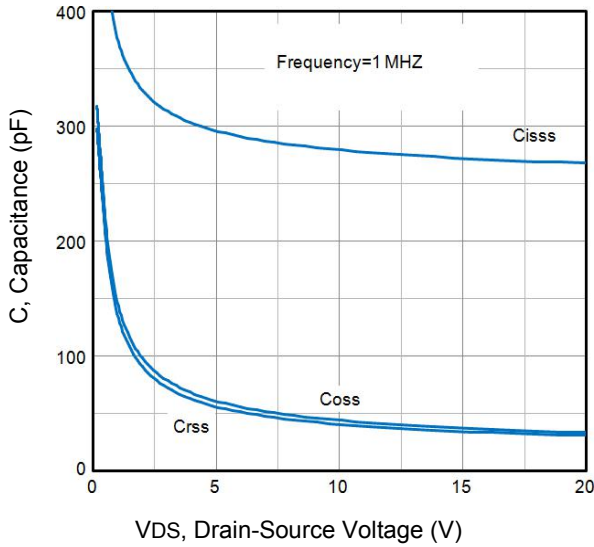


Fig7. Typical Capacitance Vs. Drain-Source Voltage

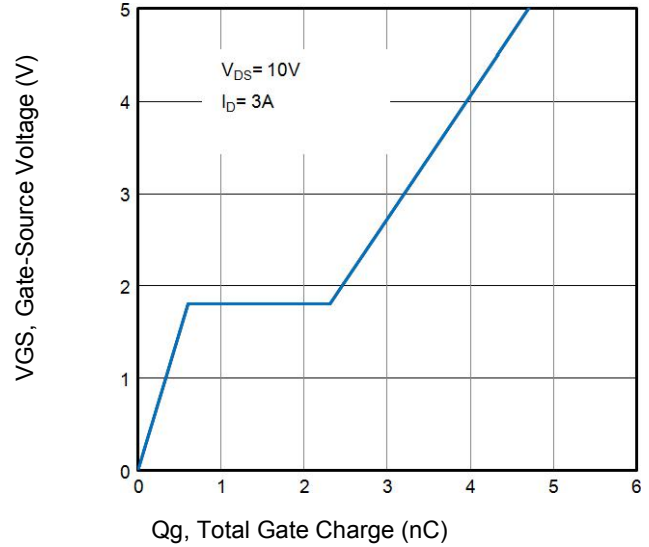


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

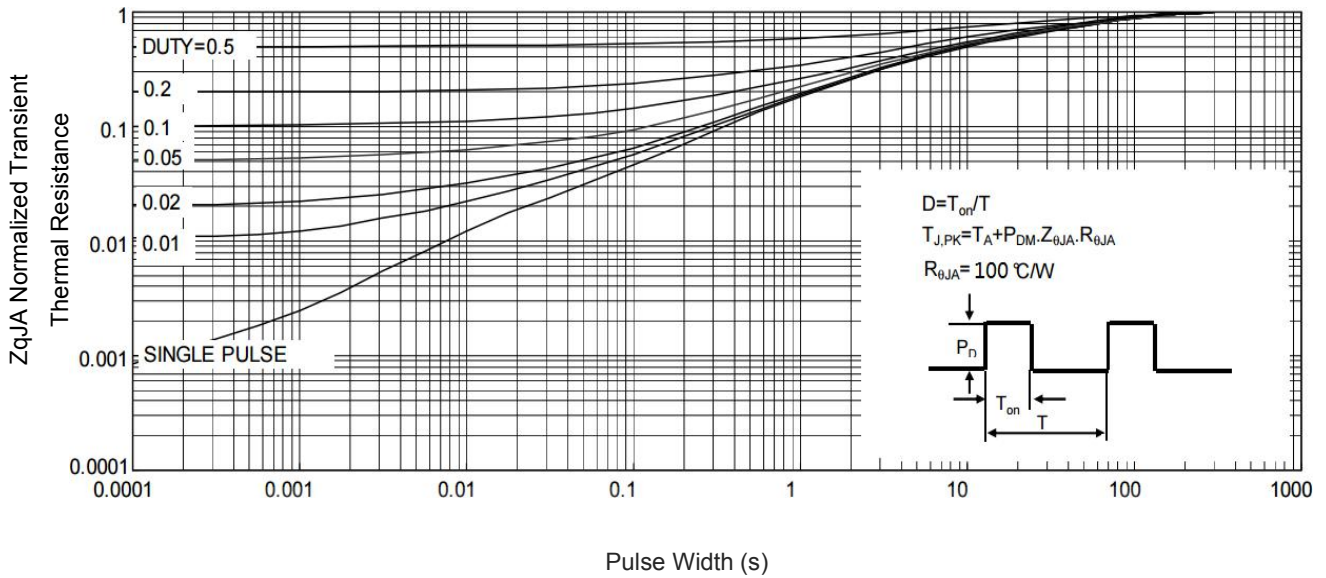


Fig9. Normalized Maximum Transient Thermal Impedance

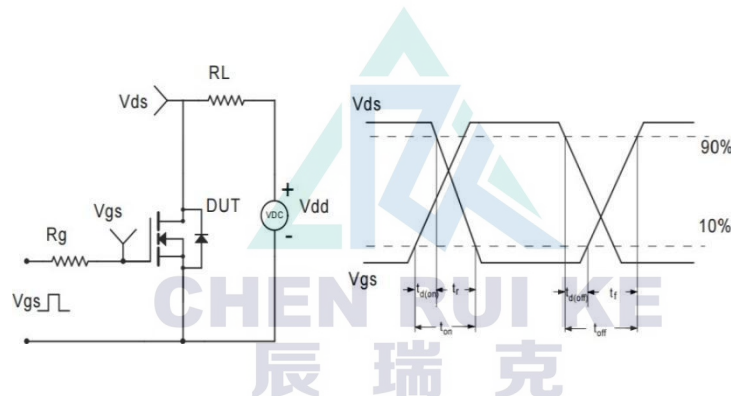
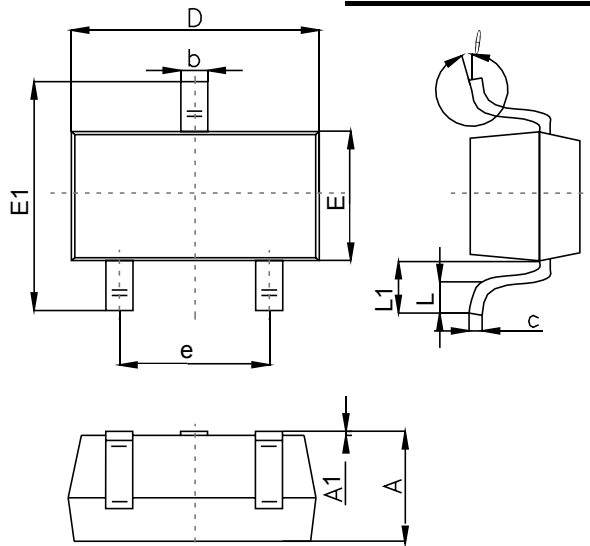


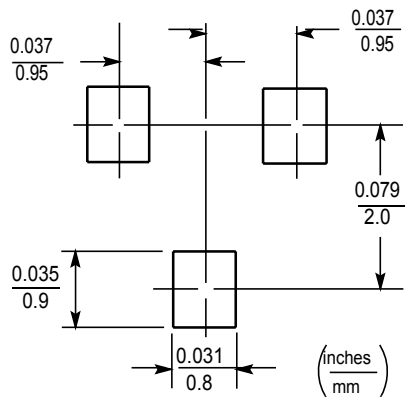
Fig10. Switching Time Test Circuit and waveforms

SOT-23 Package Outline Dimensions



Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A	1.00		1.40
A1			0.10
b	0.35		0.50
c	0.10		0.20
D	2.70	2.90	3.10
E	1.40		1.60
E1	2.4		2.80
e		1.90	
L	0.10		0.30
L1	0.4		
θ	0°		10°

Suggested Pad Layout



Note:

1. Controlling dimension: in/millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.