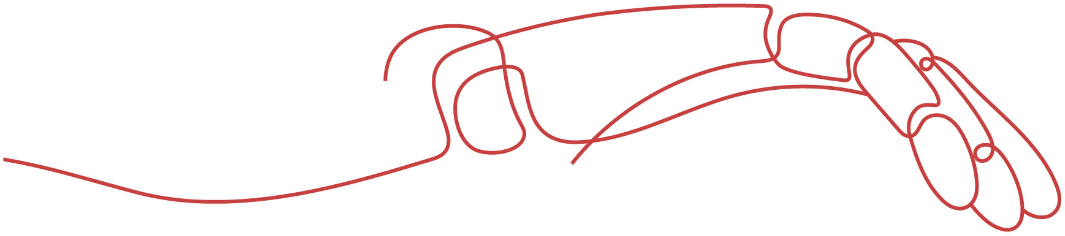


PRODUCT DATA SHEET

To learn more about JGSEMI, please visit our website at

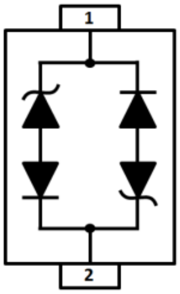
Datasheet **Resources** **Samples**

Please note: Please check the JINGAO Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.jg-semi.cn. Please email any questions regarding the system integration to JINGAO_questions@jgsemi.com.

L35L24VCB2

ESD PROTECTION DIODE

STAND-OFF VOLTAGE - 24 Volts
POWER DISSIPATION - 350 Watts



1 Cathode

2 Cathode

SOD-323

FEATURES

- Protects one power or I/O line
- Max. peak pulse power : P_{PP} = 350W at tp = 8/20 us
- Ultra Low Capacitance : 0.6pF Typical
- Low clamping voltage
- IEC 61000-4-2, level 4 (ESD), > ±30KV (air) ; > ±27KV (contact)

APPLICATION

- Ethernet - 10/100/1000 Base T
- Handheld - Wireless Systems
- USB Interface

MECHANICAL DATA

- Case material: “Green” molding compound UL flammability classification 94V-0 (No Br, Sb, Cl)
- Terminals: Lead Free Plating (Matte Tin Finish), solderable per J-STD-002 and JESD22-B/02.
- Moisture Sensitivity: Leve 1 per J-STD-020C
- Component in accordance to RoHs 2011/65/EU

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Ratings at 25°C ambient temperature unless otherwise specified.

PARAMETER	SYMBOL	VALUE	UNIT
Peak pulse power (8/20us waveform)	P_{PP}	350	W
Peak pulse current (8/20us waveform)	I_{PP}	6	A
Operating junction temperature range	T_J	-55 to +125	°C
Storage temperature range	T_{STG}	-55 to +150	°C
Soldering temperature, t max = 10s	T_L	260	°C

ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX	UNIT
Reverse standoff voltage	--	V_{DRM}	--	--	24	V
Breakdown voltage	I_t = 1mA	V_{BR}	26.7	--	--	V
Reverse leakage current	V_{DRM} = 24V	I_{RM}	--	--	1	uA
Junction capacitance	V_R = 0V, f = 1MHz,	C_J	--	0.6	0.7	pF
Clamping voltage	I_{PP} = 1A (8/20 us)	V_C	--	--	43	V
	I_{PP} = 6A (8/20 us)		--	--	58	

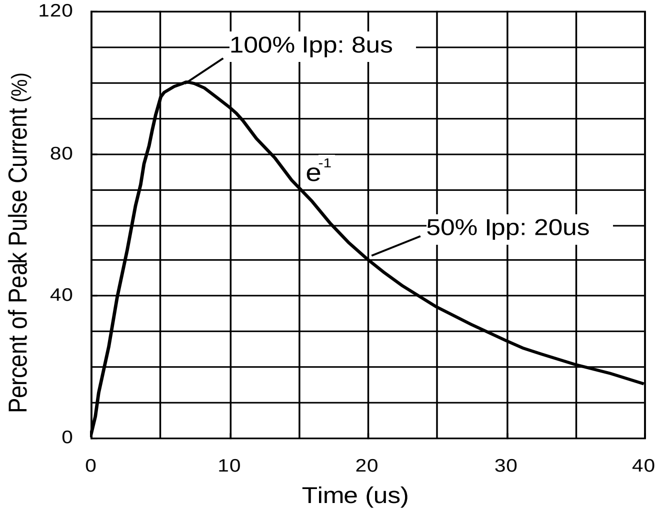


Figure 1. 8/20 us pulse waveform according to IEC 61000-4-5

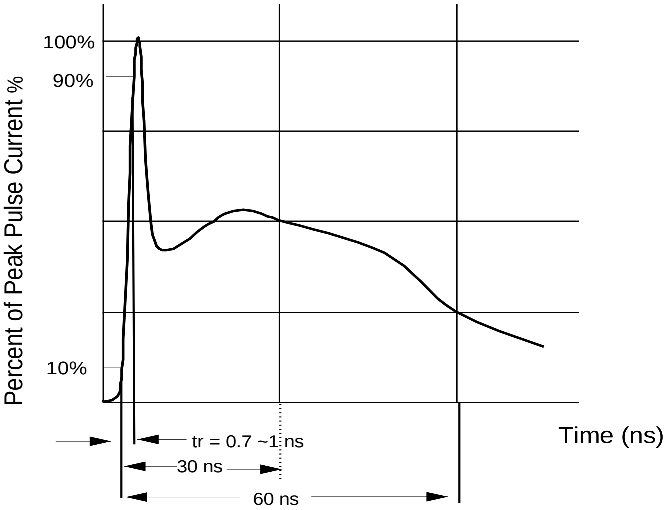


Figure 2. ESD pulse waveform according to IEC 61000-4-2

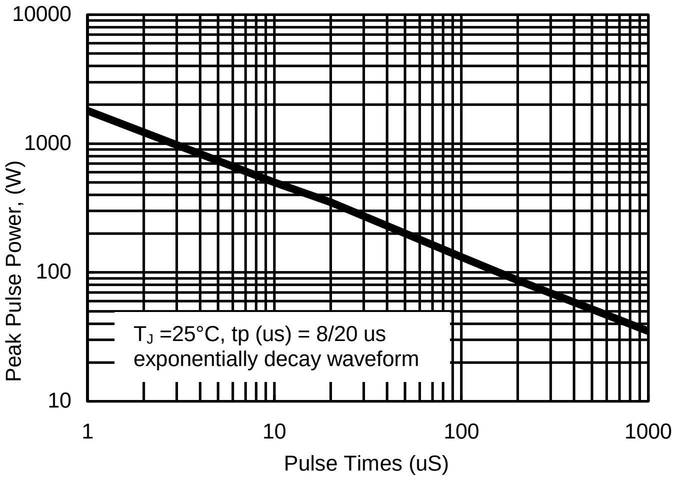


Figure 3. Power Dissipation versus Pulse Time

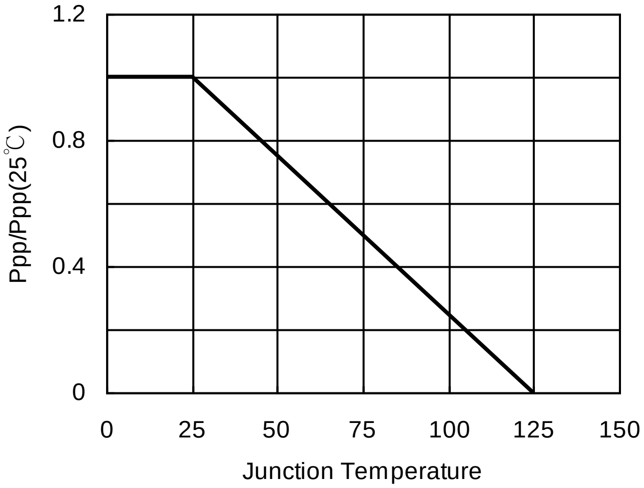


Figure 4. Peak pulse power versus TJ

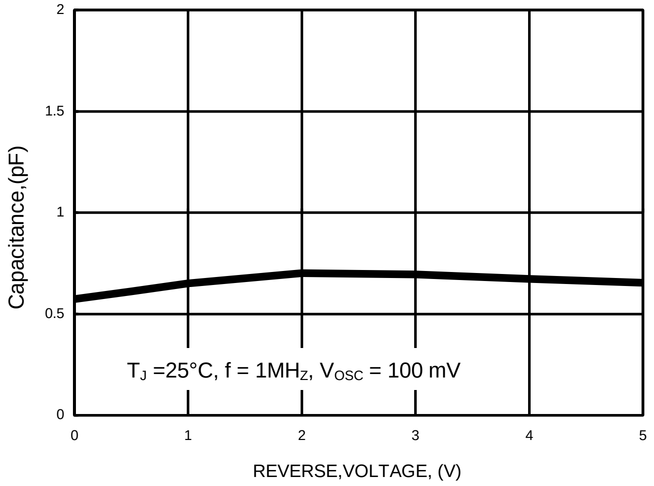


Figure 5. Typical Junction Capacitance

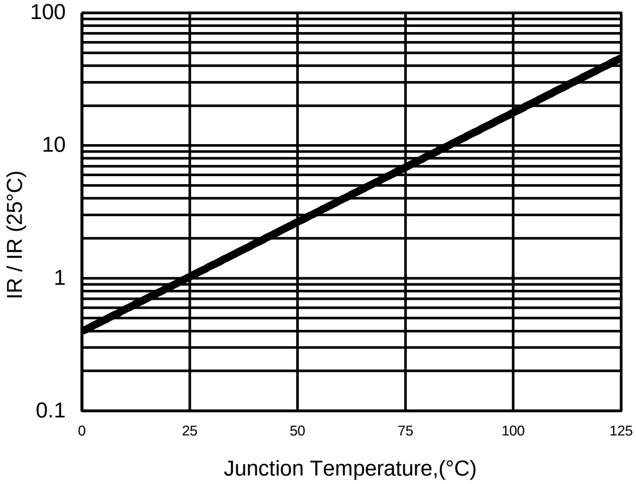


Figure 6. Reverse Leakage Current versus TJ

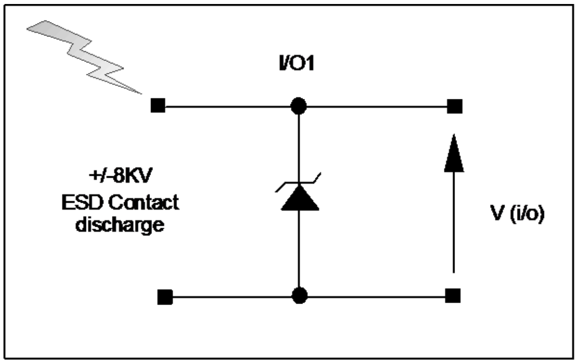


Figure 7. ESD Test Configuration

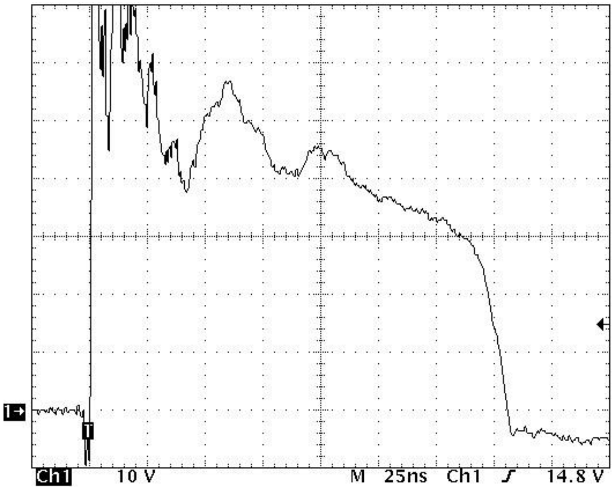


Figure 8. Clamped +8 kV ESD voltage waveform

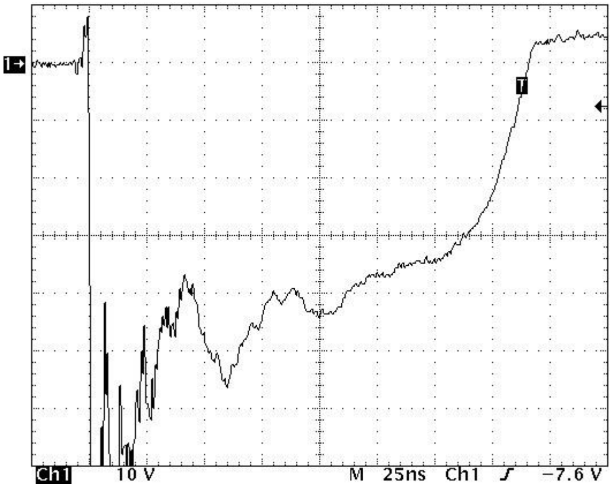
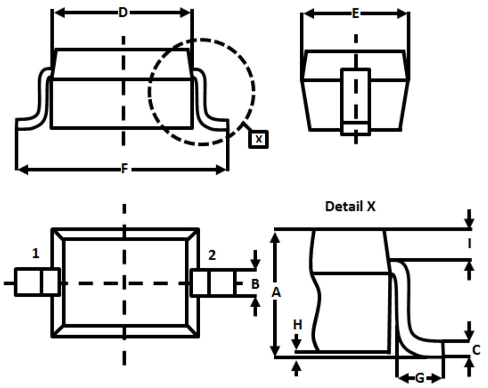


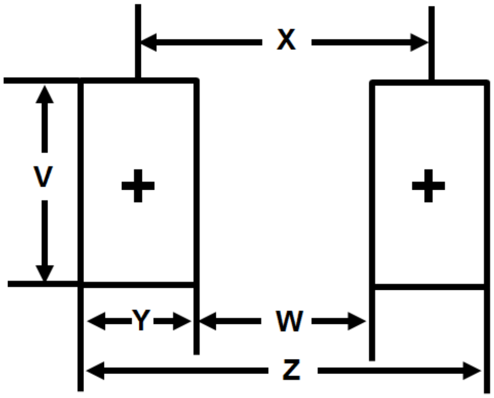
Figure 9. Clamped -8 kV ESD voltage waveform

MARKING AND PACKAGING INFORMATION



SOD-323		
DIM.	MIN.	MAX
A	0.80	1.10
B	0.25	0.40
C	0.10	0.25
D	1.60	1.80
E	1.15	1.35
F	2.30	2.70
G	0.15	0.45
H	----	0.10
I	0.15	0.25
All Dimensions in millimeter		

SOD-323 Soldering Pad Layout :



DIM.	MILLIMETERS	INCHES
Z	3.05	0.120
X	2.15	0.084
W	1.25	0.049
Y	0.90	0.035
V	0.70	0.027

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