Rail Current Measurement IC

Halogen Free

General Description

The FP136 is a wide common mode range high side rail current measurement IC. It is suitable for power systems like battery charger or switching power supply applications. It includes a differential input amplifier and a MOSFET with source output. With three external resistors, the rail current signal can be easily converted into an amplified voltage signal at the IC output pin. Also, the gain can be adjusted by changing the three external resistors values.

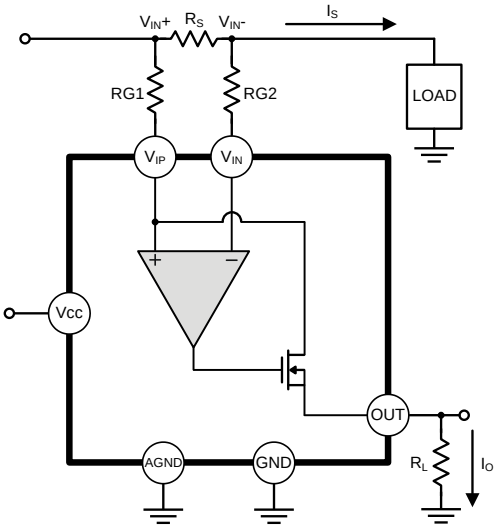
Features

- Independent Power Supply Voltage: 3.3V to 90V
- Wide Common-Mode Input Voltage: 3.3V to 90V
- Maximum Available Output Voltage (OUT Pin): 6V
- Three Resistors Gain Set-up
- Wide Temperature Range: -40℃ to +125℃
- Quiescent Current: 270μA
- Package: SOT23-6L

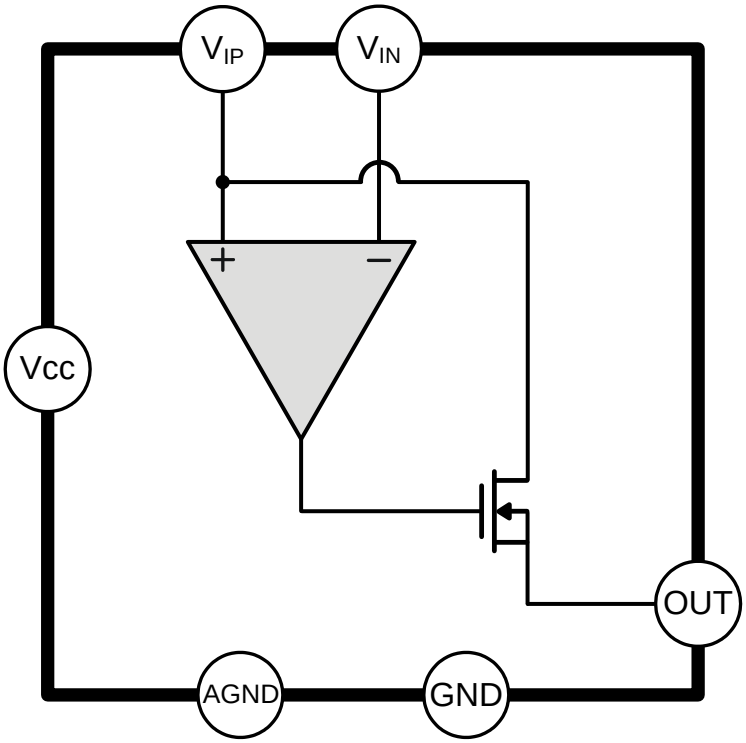
Applications

- Battery Charger
- High Side Rail Current Detector
- SPS (Adaptor)
- Current Sense Networking System

Typical Application Circuit

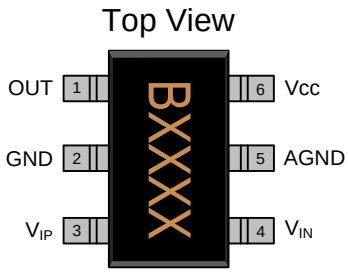


Function Block Diagram



Pin Descriptions

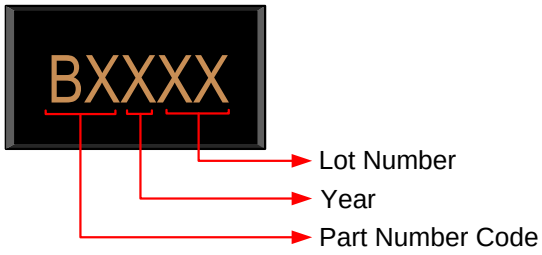
SOT23-6L



Name	No.	I / O	Description
OUT	1	O	Current Detect Output
GND	2	P	IC Ground
V_{IP}	3	I	Positive Input of Differential OPA
V_{IN}	4	I	Negative Input of Differential OPA
AGND	5	P	IC Ground
Vcc	6	P	IC Power Supply

IC Date Code Identification

SOT23-6L



Lot Number: Wafer lot number's code

Year: Production year's last digit

Part Number Code: Part number identification code for this product. It should be always "BX"

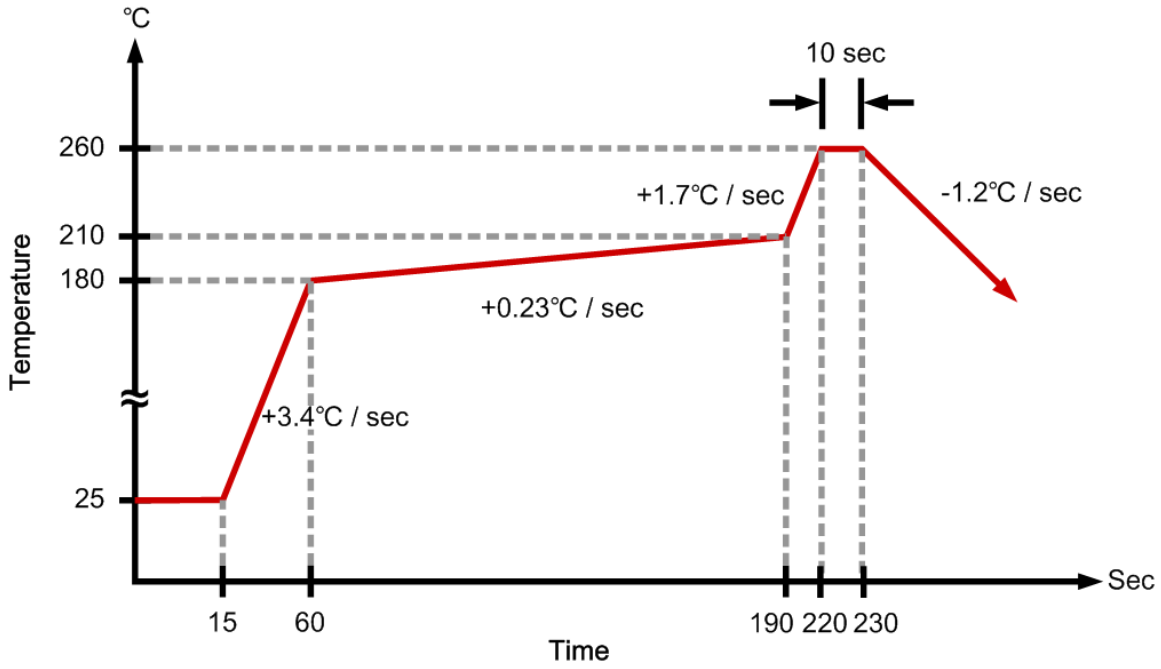
Ordering Information

Part Number	Operating Temperature	Package	MOQ	Description
FP136LR-G1	-40°C ~ +125°C	SOT23-6L	3000EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		-0.3		+95	V
Common Mode Inputs Voltage	V_{CM}		-0.3		+95	V
Differential Inputs Voltage ($V_{IP} – V_{IN}$)			-6		+6	V
OUT Voltage			-0.3		+10	V
Operating Temperature			-40		+125	°C
Storage Temperature			-55		+150	°C
Junction Temperature	T_J				+150	°C
Allowable Power Dissipation	P_D	T_A=25°C			455	mW
Junction to Ambient Thermal Resistance	θ_{JA}				+220	°C / W
Junction to Case Thermal Resistance	θ_{JC}				+130	°C / W
Lead Temperature (soldering, 10 sec)					+260	°C

IR Re-flow Soldering Curve



Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		3.3		90	V
Common-Mode Input Voltage	V_{CM}		3.3		90	V
Operating Temperature			-40		+125	°C

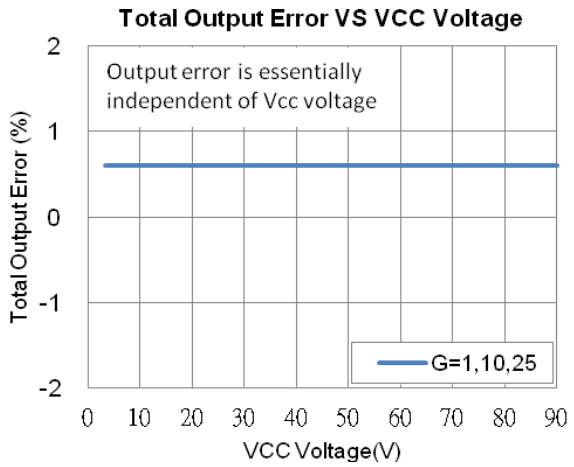
DC Electrical Characteristics

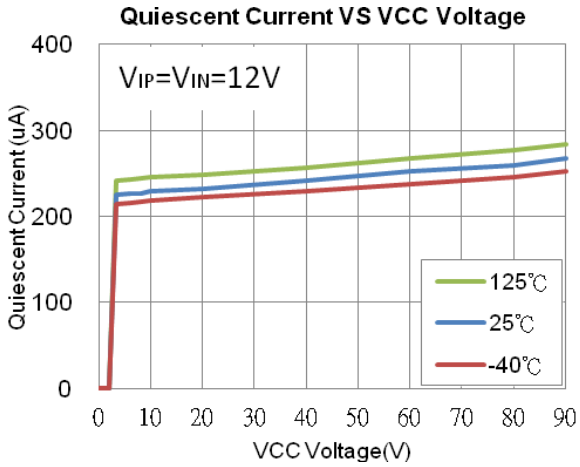
(RG1=RG2=1KΩ, R_{OUT}=25KΩ, T_A=25°C, unless otherwise noted)

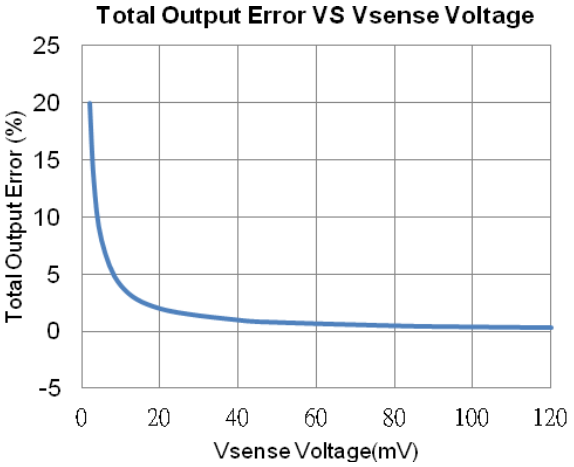
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Full Scale Sense Voltage	V_{SENSE}	$V_{SENSE}=V_{IN}+ - V_{IN}-$			500	mV
Common-Mode Input Voltage	V_{CM}		3.3		90	V
Common-Mode Rejection	CMRR			120		dB
Input Offset Voltage	V_{OFFSET}				±0.4	mV
Input Offset Voltage vs Temp.	$V_{OFFSET(TA)}$	T_{MIN} to T_{MAX}		4		μV / ℃
Input Offset Voltage vs V_{CC}	$V_{OFFSET(VCC)}$	V_{CC}=3.3V to 90V, V_{SENSE}=50mV		2.5	10	μV/V
Input Bias Current	I_{BIAS}	V_{IP},V_{IN}		5		μA
Input Bias Current	I_{BIAS}	V_{IP},V_{IN}, T_{MIN} to T_{MAX}			10	μA
Non-linearity Error	NLE	V_{SENSE}=10mV to 150mV		±0.5		%
Output Voltage	V_{OUT}	V_{SENSE}=50mV, RG1=RG2=1KΩ,RL=25KΩ	1.24	1.25	1.26	V
Output Voltage	V_{OUT}	V_{SENSE}=1mV, RG1=RG2=1KΩ,RL=100KΩ		100		mV
Maximum Output Voltage	$V_{OUT(MAX)}$	V_{SENSE}=20mV, RG1=RG2=1KΩ,RL=300KΩ	5.95	6	6.05	V
Total Output Error	TOE	V_{SENSE}=100mV			±0.8	%
Voltage Swing to V_{CC}	V_{SCC}	V_{CC}=5V, V_{IN}+=12V, V_{SENSE}=100mV, Gain=40		V_{CC}-2.2		V
Voltage Swing to V_{CM}	V_{SCM}	V_{CC}=12V, V_{IN}+=5V, V_{SENSE}=100mV, Gain=50		V_{CM}-0.5		V
Bandwidth	BW			32		KHz
Settling Time	Ts			30		μS
Output Current	I_{OUT}		0.5			mA
Operating Voltage Range	V_{CC}		3.3		90	V
Under Voltage Lockout	V_{UVLO}			2.7		V
Quiescent Current	I_{CC}	V_{SENSE}=0, V_{CC} =90V		270		μA

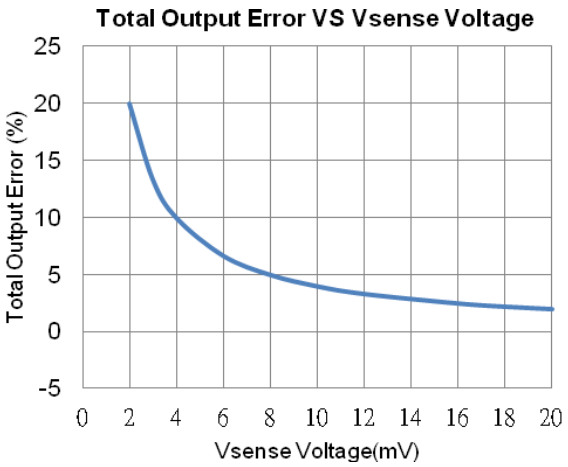
Typical Operating Characteristics

(VCC=12V,V_{IP}=V_{IN}=12V, T_A=25℃, unless otherwise specified)

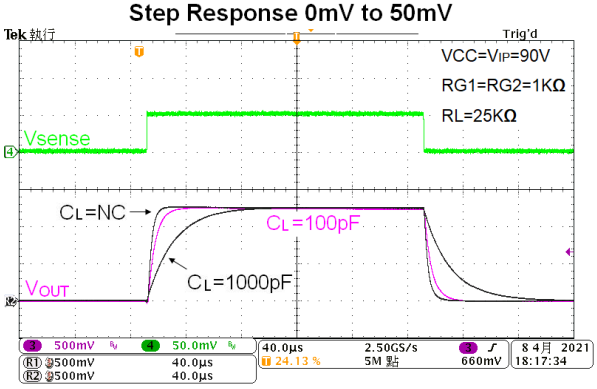




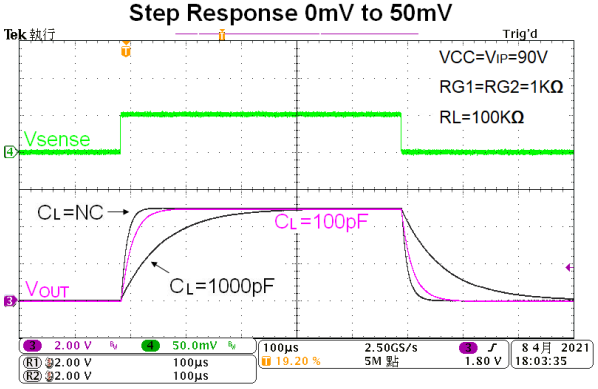




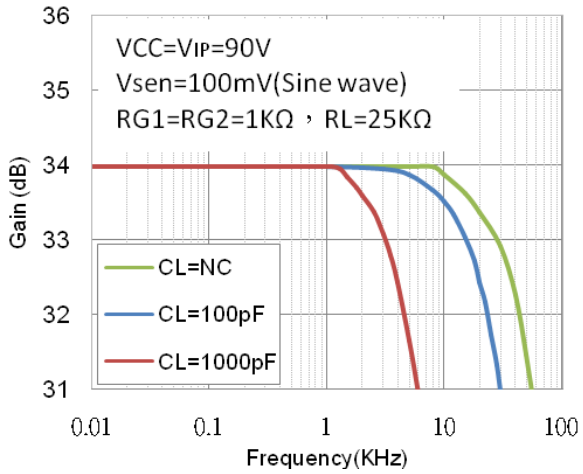
Step Response 0mV to 50mV



Step Response 0mV to 50mV



Gain VS Frequency



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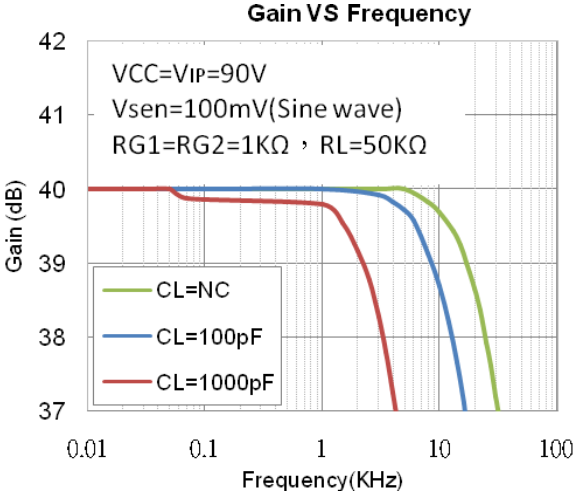

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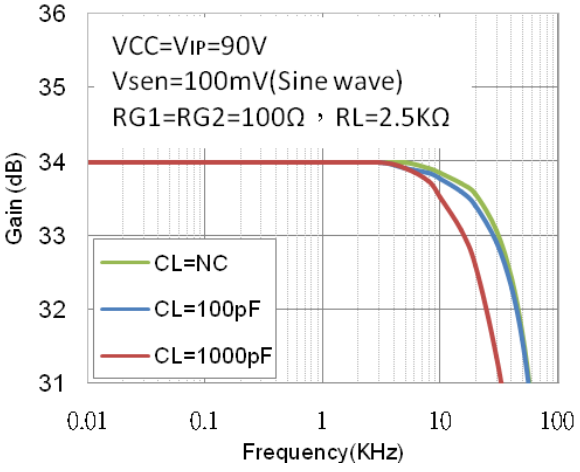
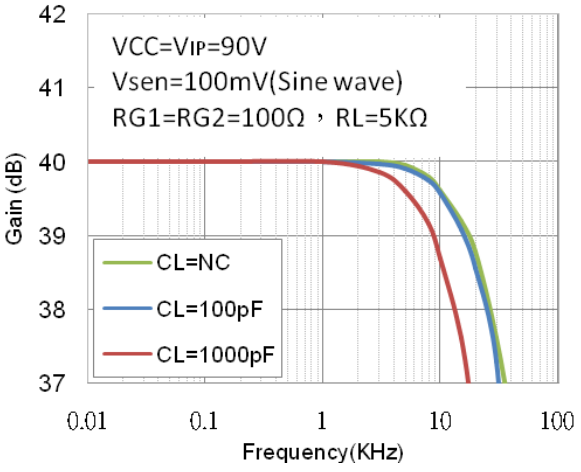


Gain VS Frequency



Function Description

Figure 1 shows the FP136 basic application circuit, the load current (I_S) flows from power supply and generates a voltage difference (V_{IN}+ - V_{IN}-) at the sense resistor (R_S). Assume internal MOSFET Drain current is same as Source current (I_O) and V_{IP} is very close V_{IN}, the FP136 transfer function is:

$$I_O = \frac{V_{IN}^{+} - V_{IN}^{-}}{RG1} \quad \text{----- (1)}$$

In the circuit of Figure 1, the (V_{IN}+ - V_{IN}-), is equal to $I_S \times R_S$ and the output voltage (OUT) is equal to I_O x R_L. The final transfer function for rail current measurement in this application is:

$$V_{OUT} = G \times I_S \times R_S \quad \text{----- (2)}$$

$$G = R_L / RG1 \quad \text{----- (3)}$$

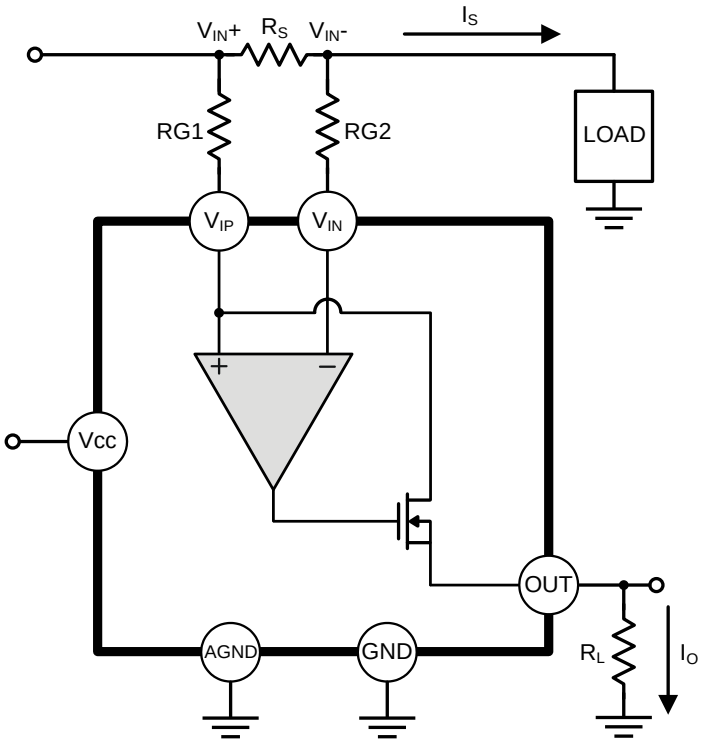


Figure 1 Current Measurement Circuit

Note:

1. The (RG1=RG2) must be less than or equal to 1KΩ, which can reduce output deviation.
2. The minimum operating voltages of V_{CC}, V_{IP} and V_{IN} are 3.3V. If these supply voltages are lower than 3.3V, the transfer function at output of FP136 is no longer applicable.
3. The maximum voltage difference between V_{IP} and V_{IN} is ±6V. If the (V_{IP}-V_{IN}) is over ±6V, it will result in damage.
4. The maximum amplified output voltage is 6V.
5. Capacitors cannot be connected from VIP pin and VIN pin to ground.

Figure 2 shows a simple method to delay the converting time. When a transient voltage happens at sense resistor (R_S), the IC would change sourcing current (I_O) to the output and generate a voltage change at the output. The RC circuit will delay a time during output change.

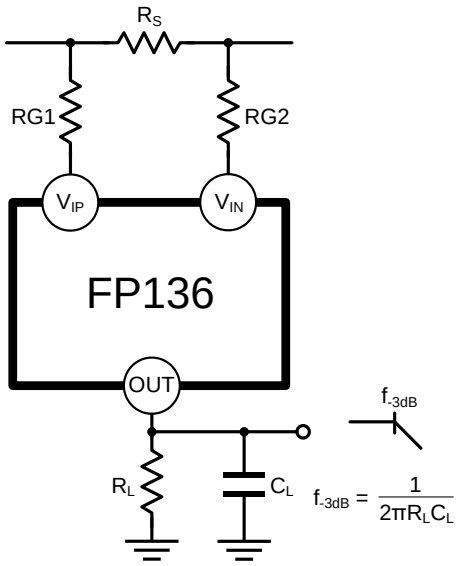


Figure 2 Output R-C Delay Circuit

Figure 3 shows a detection circuit using 1.25V reference comparator. At initial, the non-inverting input of the comparator is 1.25V which is higher than inverting input. The comparator's output signal is high. Once the IC output voltage is higher than 1.25V, the comparator's output will change to low.

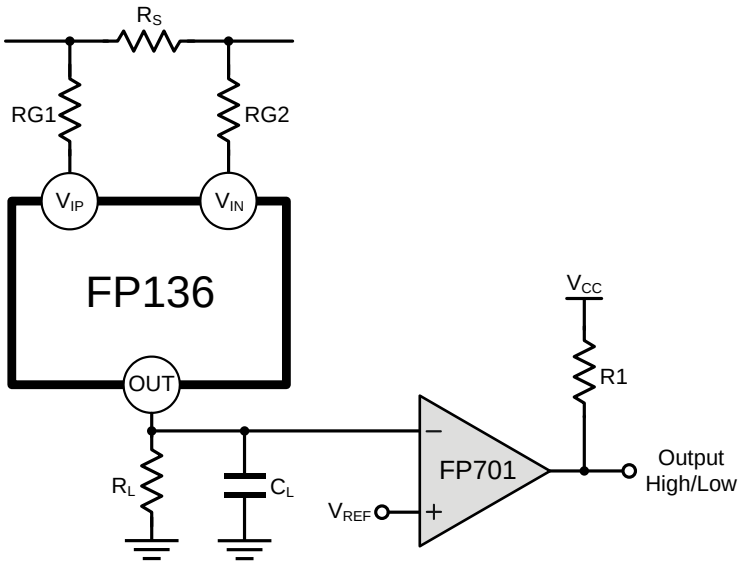


Figure 3 Comparator Detection Circuit

Figure 4 shows a buffer output circuit using an operational amplifier. When devices connect to OUT pin directly, its impedance is connected in parallel with the gain setting resistor R_L. If the impedance of devices is lower, the parallel impedance combination will affect the gain of system, which causes inaccurate output voltage. To place a buffer amplifier between OUT pin and device is a simple method to solve the impact of impedance.

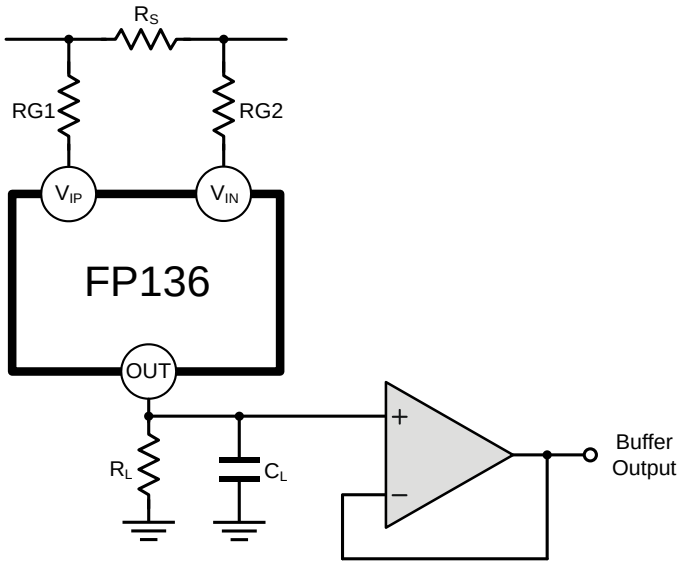
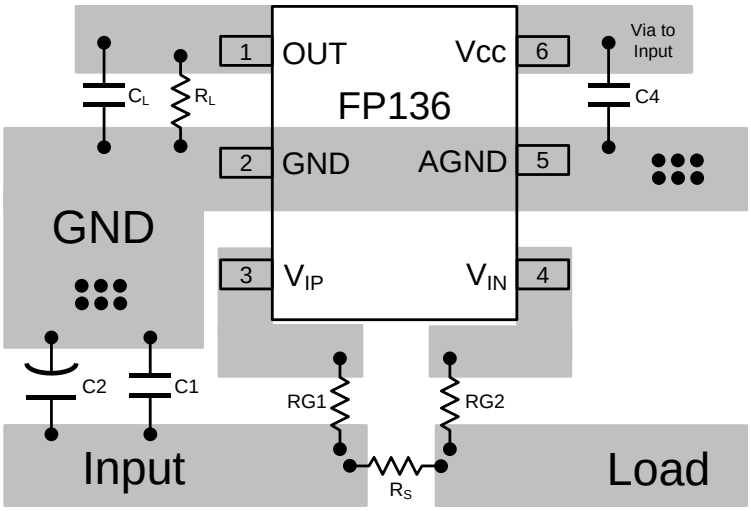


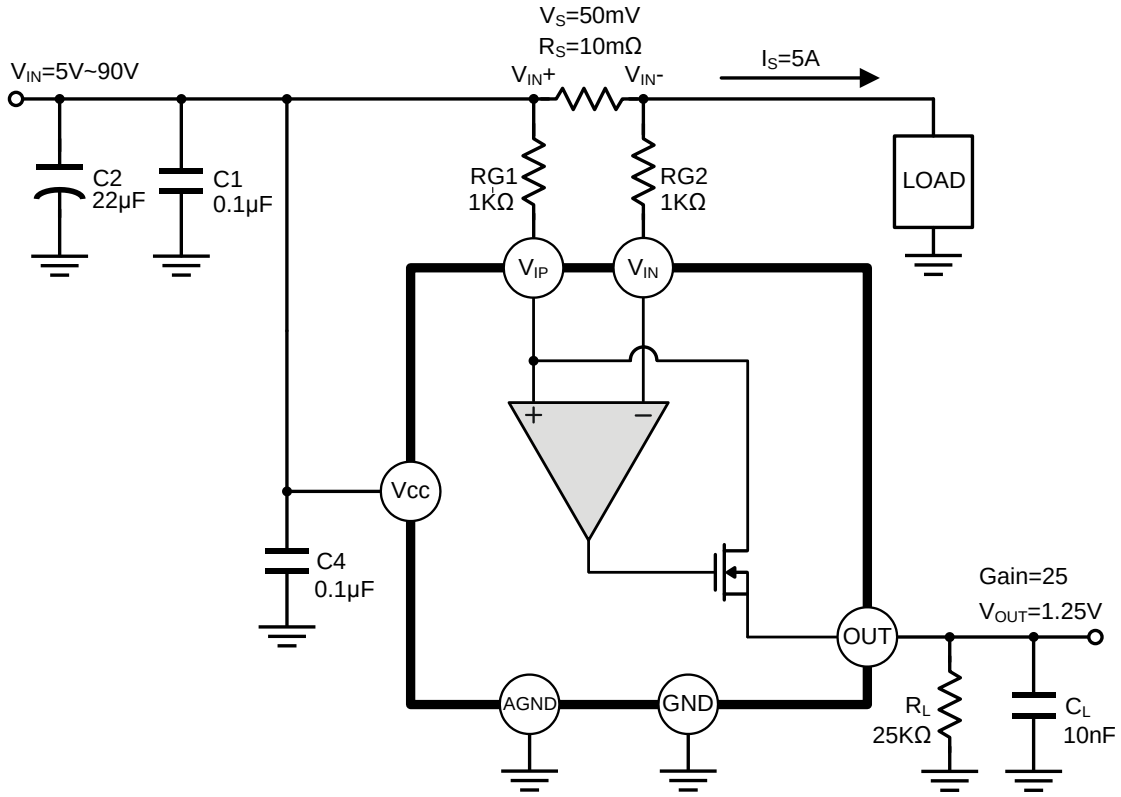
Figure 4 Buffer Output Circuit

Layout Considerations

1. RG1 and RG2 must be connected to R_S, V_{IP} and V_{IN} directly as closely as possible.
2. Place C4 nearby Vcc pin as closely as possible to maintain Vcc voltage steady and filter noise.
3. R_L and C_L are connected to OUT and GND pin directly and as closely as possible.

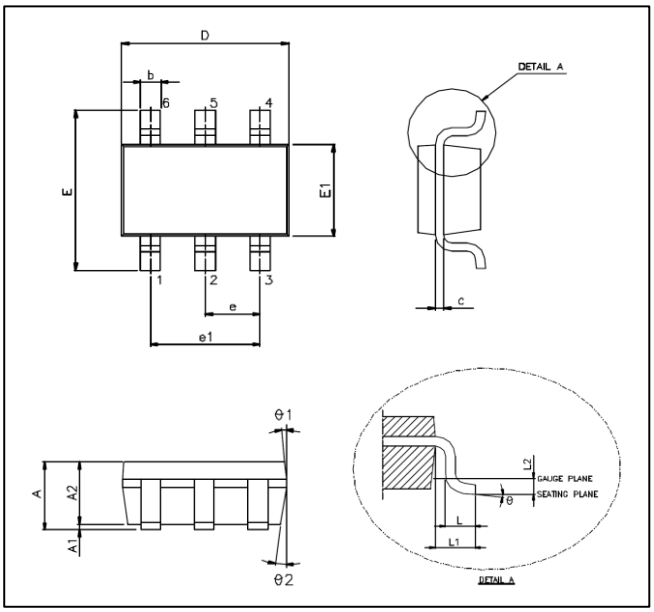


Typical Application



Package Outline

SOT23-6L



Unit: mm

Symbols	Min. (mm)	Max. (mm)
A	0.950	1.450
A1	0.050	0.150
A2	0.900	1.300
b	0.300	0.500
c	0.080	0.220
D	2.900 BSC	
E	2.800 BSC	
E1	1.600 BSC	
e	0.950 BSC	
e1	1.900 BSC	
L	0.300	0.600
L1	0.600 REF	
L2	0.250 BSC	
θ°	0°	8°
θ1°	3°	7°
θ2°	6°	15°

Note:

1. Package dimensions are in compliance with JEDEC outline: MO-178 AB.
2. Dimension “D” does not include molding flash, protrusions or gate burrs.
3. Dimension “E1” does not include inter-lead flash or protrusions.