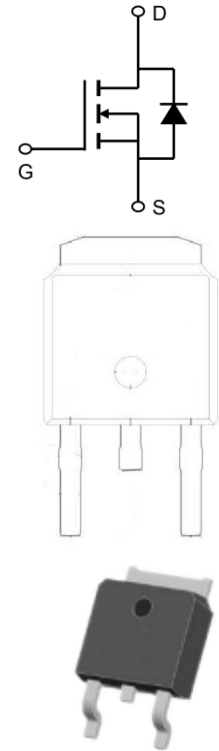


100V N-Channel Enhancement Mode MOSFET

Description

The 30N10 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

$V_{DS} = 100V$ $I_D = 30A$

$R_{DS(ON)} < 47m\Omega$ @ $V_{GS}=10V$

Application

Battery protection

Load switch

Uninterruptible power supply

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
30N10	TO-252-3L	30N10 XXX YYYY	2500

Absolute Maximum Ratings $T_c=25^\circ C$ unless otherwise noted

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_c=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	30	A
$I_D@T_c=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	13.5	A
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	4.2	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	3.4	A
I_{DM}	Pulsed Drain Current ²	45	A
EAS	Single Pulse Avalanche Energy ³	36.5	mJ
I_{AS}	Avalanche Current	27	A
$P_D@T_c=25^\circ C$	Total Power Dissipation ⁴	52.1	W
$P_D@T_A=25^\circ C$	Total Power Dissipation ⁴	2	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	2.4	$^\circ C/W$

100V N-Channel Enhancement Mode MOSFET

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	100	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.098	---	V/°C
R _{DS(on)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =20A	---	38	47	mΩ
		V _{GS} =4.5V, I _D =15A	---	40	50	
V _{GS(th)}	Gate Threshold Voltage		1.3	---	2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient	V _{GS} =V _{DS} , I _D =250uA	---	-5.52	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =80V, V _{GS} =0V, T _J =25°C	---	---	10	uA
		V _{DS} =80V, V _{GS} =0V, T _J =55°C	---	---	100	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =20A	---	28.7	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	1.6	3.2	Ω
Q _g	Total Gate Charge (10V)		---	60	84	nC
Q _{gs}	Gate-Source Charge	V _{DS} =80V, V _{GS} =10V, I _D =20A	---	9.7	14	
Q _{gd}	Gate-Drain Charge		---	11.8	16.5	
T _{d(on)}	Turn-On Delay Time		---	10.4	21	ns
T _r	Rise Time	V _{DD} =50V, V _{GS} =10V, R _G =3.3Ω	---	46	83	
T _{d(off)}	Turn-Off Delay Time	I _D =20A	---	54	108	
T _f	Fall Time		---	10	20	
C _{iss}	Input Capacitance		---	3848	5387	pF
C _{oss}	Output Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	137	192	
C _{rss}	Reverse Transfer Capacitance		---	82	115	
I _S	Continuous Source Current ^{1,5}		---	---	22	A
I _{SM}	Pulsed Source Current ^{2,5}	V _G =V _D =0V, Force Current	---	---	45	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.2	V
t _{rr}	Reverse Recovery Time	I _F =20A, dI/dt=100A/μs, T _J =25°C	---	30	---	nS
Q _{rr}	Reverse Recovery Charge		---	37	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3.The EAS data shows Max. rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=27A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

100V N-Channel Enhancement Mode MOSFET

Typical Characteristics

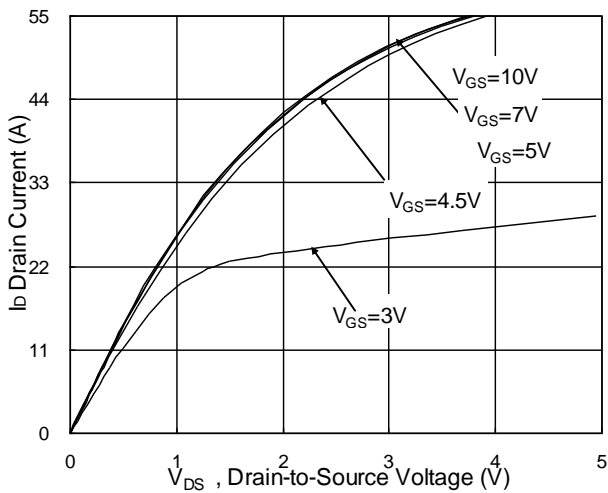


Fig.1 Typical Output Characteristics

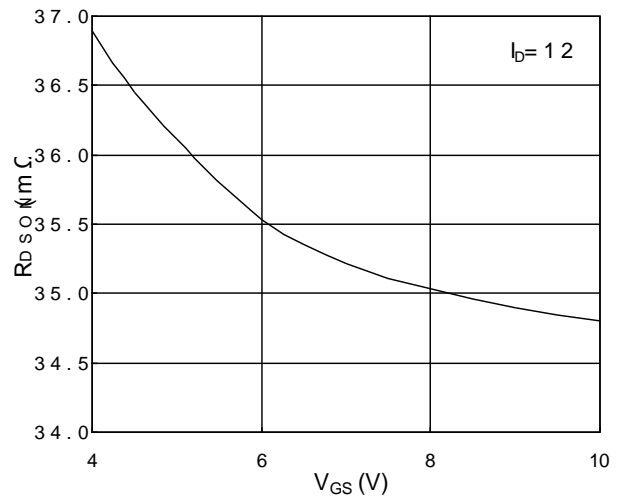


Fig.2 On-Resistance vs. Gate-Source

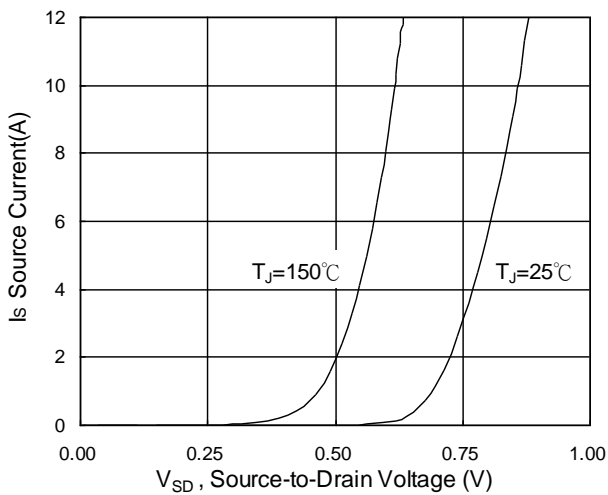


Fig.3 Forward Characteristics Of Reverse

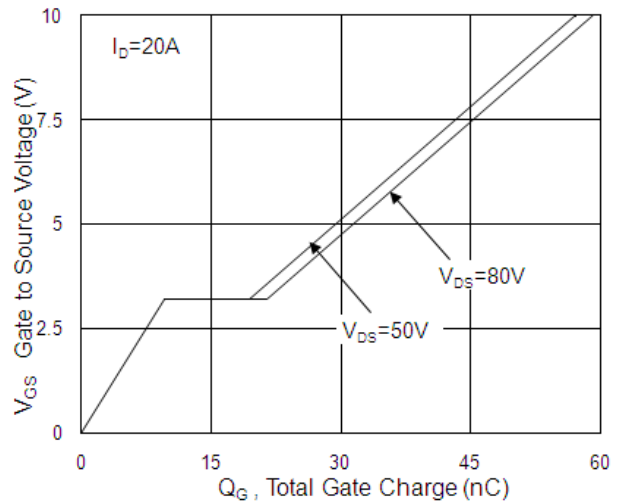


Fig.4 Gate-Charge Characteristics

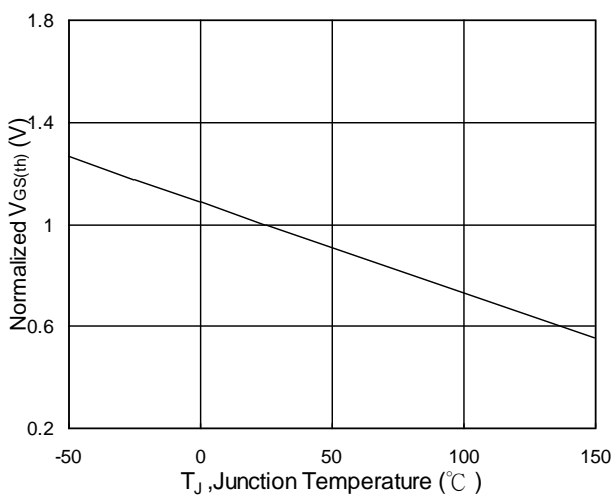


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

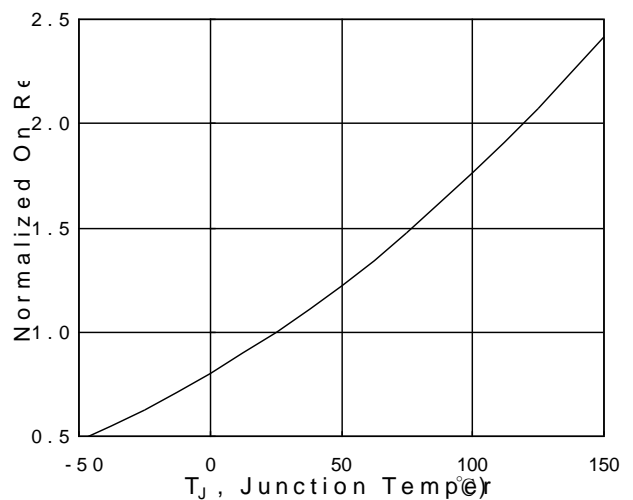


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

100V N-Channel Enhancement Mode MOSFET

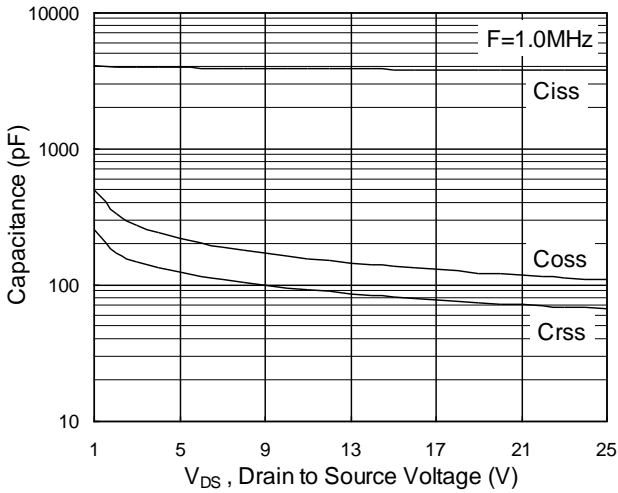


Fig.7 Capacitance

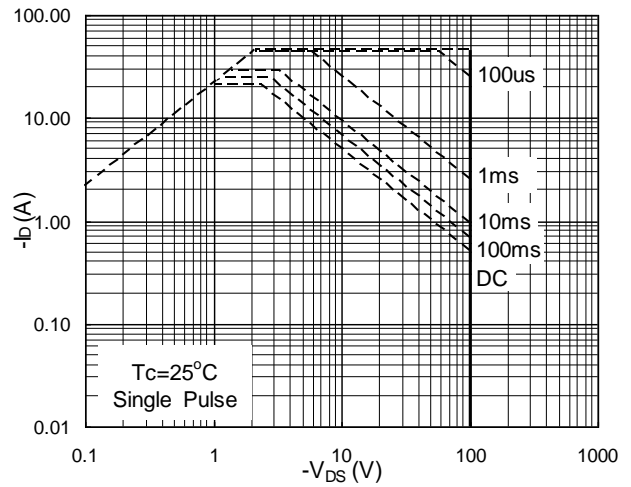


Fig.8 Safe Operating Area

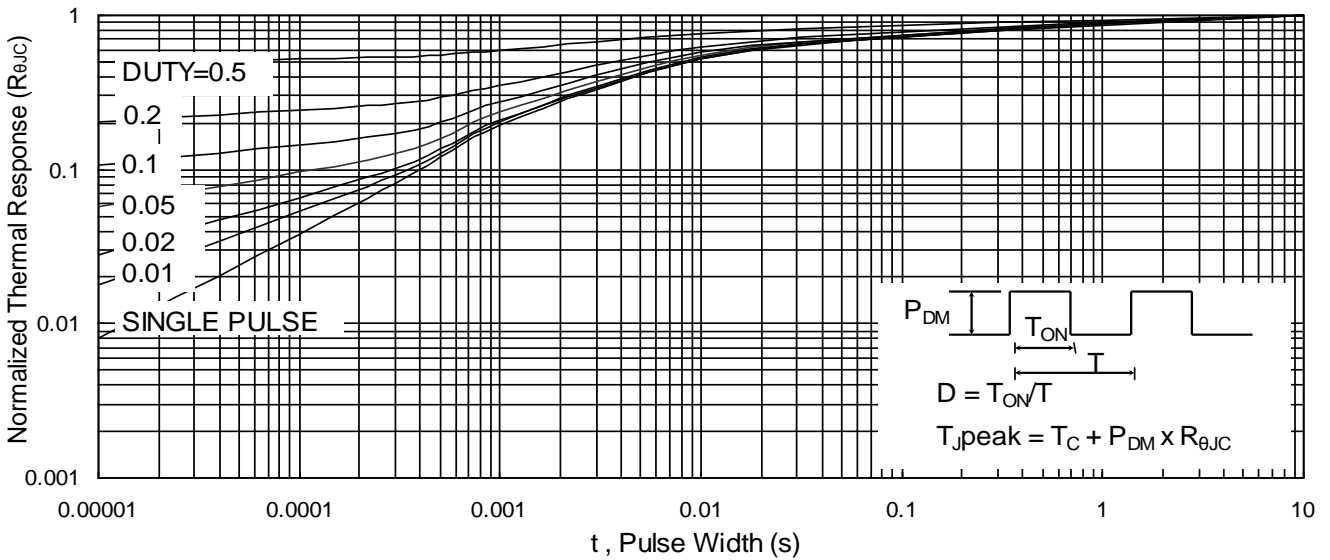


Fig.9 Normalized Maximum Transient Thermal Impedance

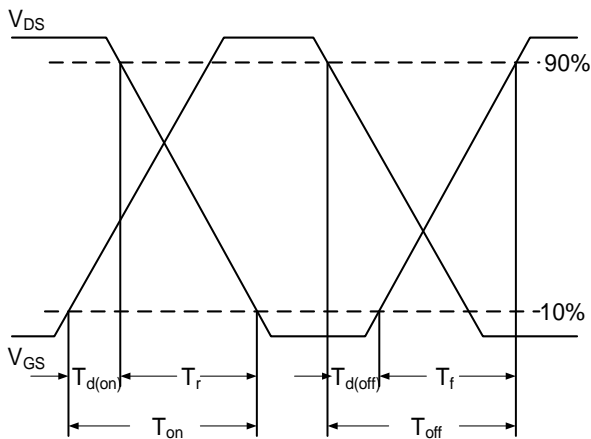


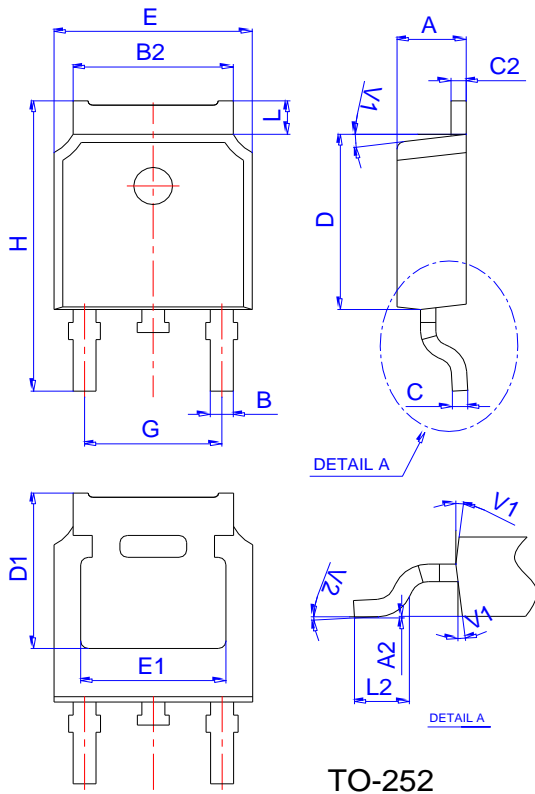
Fig.10 Switching Time Waveform



Fig.11 Unclamped Inductive Switching Waveform

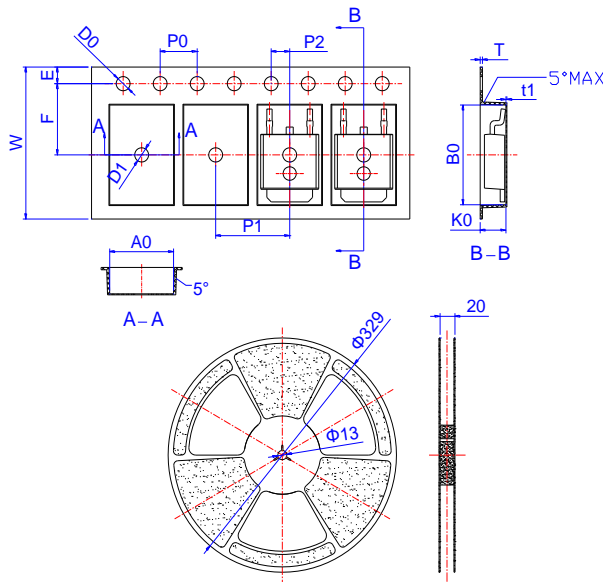
100V N-Channel Enhancement Mode MOSFET

Package Mechanical Data



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583