



CD4021

8-bit Static Shift Register

Product Specification

Specification Revision History:

Version	Date	Description
2022-06-A1	2022-06	New
2023-04-B1	2023-04	Update the template



Contents

1、General Description.....	1
2、Block Diagram And Pin Description	3
2.1、Block Diagram	3
2.2、Pin Configurations.....	4
2.3、Pin Description.....	4
2.4、Function Table.....	5
3、Electrical Parameter	5
3.1、Absolute Maximum Ratings.....	5
3.2、Recommended Operating Conditions	6
3.3、Electrical Characteristics.....	6
3.3.1、DC Characteristics 1	6
3.3.2、DC Characteristics 2.....	7
3.3.3、AC Characteristics.....	8
4、Testing Circuit	9
4.1、AC Testing Circuit	9
4.2、AC Testing Waveforms.....	9
4.3、Measurement Points	10
4.4、Test Data	10
5、Package Information	11
5.1、DIP16	11
5.2、SOP16	12
5.3、TSSOP16.....	13
6、Statements And Notes	14
6.1、The name and content of Hazardous substances or Elements in the product.....	14
6.2、Notes	14



1、General Description

The CD4021 is an 8-bit static shift register (parallel-to-serial converter) with a synchronous serial data input (DS), a clock input (CP), an asynchronous active HIGH parallel load input (PL), eight asynchronous parallel data inputs (D0 to D7) and buffered parallel outputs from the last three stages (Q5 to Q7).

Each register stage is a D-type master-slave flip-flop with a set direct (SD) and clear direct (CD) input. Information on D0 to D7 is asynchronously loaded into the register while PL is HIGH, independent of CP and DS. When PL is LOW, data on DS is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of CP. Schmitt trigger action makes the clock input highly tolerant of slower rise and fall times.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

Features:

- Tolerant of slower rise and fall times
- Fully static operation
- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to +125°C
- Package information: DIP16/SOP16/TSSOP16

**Ordering Information:****Tube packing specifications:**

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
CD4021DA16.TB	DIP16	CD4021	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing:2.54mm
CD4021SA16.TB	SOP16	CD4021	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
CD4021TA16.TB	TSSOP16	CD4021	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
CD4021SA16.TR	SOP16	CD4021	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
CD4021TA16.TR	TSSOP16	CD4021	5000PCS/reel	10000PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.



2、Block Diagram And Pin Description

2.1、Block Diagram

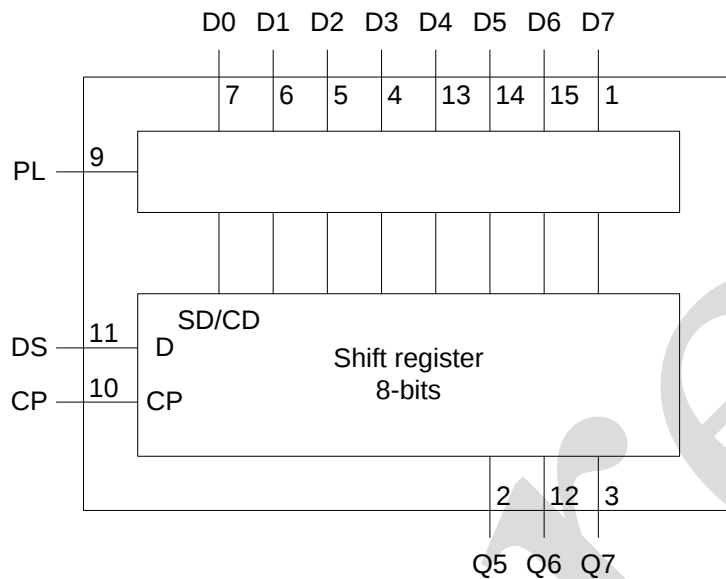


Figure 1. Functional diagram

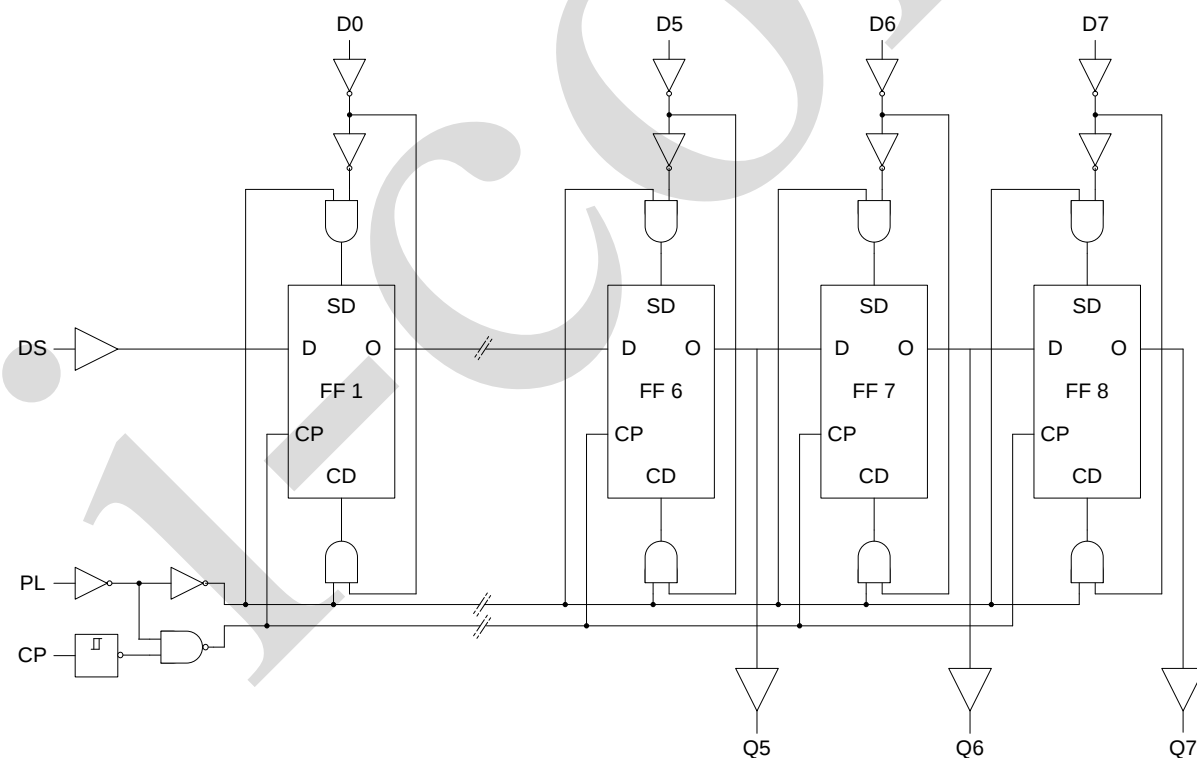
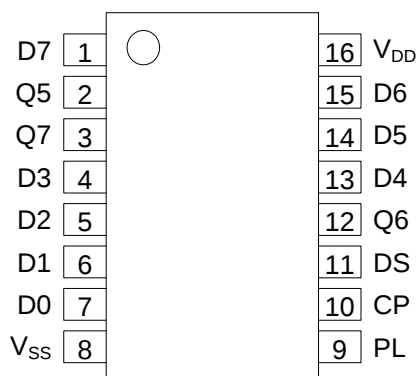


Figure 2. Logic diagram



2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	D7	parallel data input
2	Q5	buffered parallel output from the last three stages
3	Q7	buffered parallel output from the last three stages
4	D3	parallel data input
5	D2	parallel data input
6	D1	parallel data input
7	D0	parallel data input
8	V _{SS}	ground supply voltage
9	PL	parallel load input
10	CP	clock input (LOW-to-HIGH edge-triggered)
11	DS	serial data input
12	Q6	buffered parallel output from the last three stages
13	D4	parallel data input
14	D5	parallel data input
15	D6	parallel data input
16	V _{DD}	supply voltage

**2.4、Function Table**

Number of clock transitions	Inputs			Outputs		
	CP	DS	PL	Q5	Q6	Q7
Serial operation						
1	↑	data 1	L	X	X	X
2	↑	data 2	L	X	X	X
3	↑	data 3	L	X	X	X
6	↑	X	L	data 1	X	X
7	↑	X	L	data 2	data 1	X
8	↑	X	L	data 3	data 2	data 1
	↓	X	L	no change	no change	no change
Parallel operation						
	X	X	H	D5	D6	D7

Note:

[1] H=HIGH voltage level; L=LOW voltage level; X=don't care;
 ↑=LOW to HIGH clock transition; ↓=HIGH to LOW clock transition;
 data n=data (HIGH or LOW) on the DS input at the nth ↑ CP transition.

3、Electrical Parameter**3.1、Absolute Maximum Ratings**(T_{amb}=25℃, unless otherwise specified)

Characteristic	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V _{DD}	-		-0.5	+18	V
input clamping current	I _{IK}	V _I <-0.5V or V _I >V _{DD} +0.5V		-	±10	mA
input voltage	V _I	-		-0.5	V _{DD} +0.5	V
output clamping current	I _{OK}	V _I <-0.5V or V _I >V _{DD} +0.5V		-	±10	mA
input/output current	I _{I/O}	-		-	±10	mA
supply current	I _{DD}	-		-	50	mA
storage temperature	T _{stg}	-		-65	+150	℃
total power dissipation	P _{tot}	-		500		mW
power dissipation	P _D	per output		100		mW
soldering temperature	T _L	10s	DIP	245		℃
			SOP/TSSOP	260		℃



3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	-	15	V
input voltage	V_I	-	0	-	V_{DD}	V
operating temperature	T_{amb}	-	-40	-	+125	°C

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions (V)			$T_{amb}=25^{\circ}\text{C}$			Unit
		V_O	V_{IN}	V_{DD}	Min.	Typ.	Max.	
supply current	I_{DD}	-	0, 5	5	-	-	5	uA
		-	0, 10	10	-	-	10	uA
		-	0, 15	15	-	-	20	uA
LOW-level output current	I_{OL}	0.4	0, 5	5	0.5	-	-	mA
		0.5	0, 10	10	1.3	-	-	mA
		1.5	0, 15	15	3.4	-	-	mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-	-	-0.5	mA
		2.5	0, 5	5	-	-	-1.4	mA
		9.5	0, 10	10	-	-	-1.3	mA
		13.5	0, 15	15	-	-	-3.4	mA
LOW-level output voltage	V_{OL}	-	0, 5	5	-	-	0.05	V
		-	0, 10	10	-	-	0.05	V
		-	0, 15	15	-	-	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	-	-	V
		-	0, 10	10	9.95	-	-	V
		-	0, 15	15	14.95	-	-	V
LOW-level input voltage	V_{IL}	4.5	-	5	-	-	1.5	V
		9	-	10	-	-	3	V
		13.5	-	15	-	-	4	V
HIGH-level input voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	V
		1, 9	-	10	7	-	-	V
		1.5, 13.5	-	15	11	-	-	V
input leakage current	I_I	-	0, 15	15	-	-	± 1.0	uA
input capacitance	C_I	-	-	-	-	-	7.5	pF



3.3.2、DC Characteristics 2

($T_{amb}=-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions (V)			$T_{amb}=-40^{\circ}\text{C}$		$T_{amb}=+85^{\circ}\text{C}$		$T_{amb}=+125^{\circ}\text{C}$		Unit
		V_O	V_{IN}	V_{DD}	Min.	Max.	Min.	Max.	Min.	Max.	
supply current	I_{DD}	-	0, 5	5	-	5	-	150	-	15	μA
		-	0, 10	10	-	10	-	300	-	300	μA
		-	0, 15	15	-	20	-	600	-	600	μA
LOW-level output current	I_{OL}	0.4	0, 5	5	0.64	-	0.36	-	0.36	-	mA
		0.5	0, 10	10	1.6	-	0.9	-	0.9	-	mA
		1.5	0, 15	15	4.2	-	2.4	-	2.4	-	mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-	-0.64	-	-0.36	-	-0.36	mA
		2.5	0, 5	5	-	-1.7	-	-1.1	-	-1.1	mA
		9.5	0, 10	10	-	-1.6	-	-0.9	-	-0.9	mA
		13.5	0, 15	15	-	-4.2	-	-2.4	-	-2.4	mA
LOW-level output voltage	V_{OL}	-	0, 5	5	-	0.05	-	0.05	-	0.05	V
		-	0, 10	10	-	0.05	-	0.05	-	0.05	V
		-	0, 15	15	-	0.05	-	0.05	-	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	-	4.95	-	4.95	-	V
		-	0, 10	10	9.95	-	9.95	-	9.95	-	V
		-	0, 15	15	14.95	-	14.95	-	14.95	-	V
LOW-level input voltage	V_{IL}	4.5	-	5	-	1.5	-	1.5	-	1.5	V
		9	-	10	-	3	-	3	-	3	V
		13.5	-	15	-	4	-	4	-	4	V
HIGH-level input voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	7	-	V
		1.5, 13.5	-	15	11	-	11	-	11	-	V
input leakage current	I_I	-	0, 15	15	-	± 0.1	-	± 1.0	-	± 1.0	μA

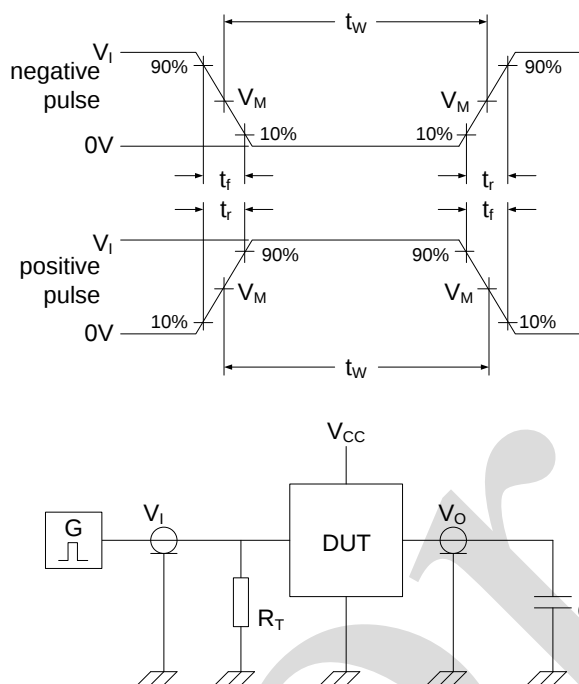
**3.3.3、AC Characteristics**(T_{amb}=25°C, V_{SS}=0V, unless otherwise specified)

Parameter	Symbol	Conditions	V _{DD}	Min.	Typ.	Max.	Unit
HIGH to LOW propagation delay	t _{PHL}	CP to Qn; see Figure 4	5	-	125	250	ns
			10	-	55	110	ns
			15	-	40	80	ns
		PL to Qn; see Figure 4	5	-	135	240	ns
			10	-	78	110	ns
			15	-	65	80	ns
LOW to HIGH propagation delay	t _{PLH}	CP to Qn; see Figure 4	5	-	115	230	ns
			10	-	50	100	ns
			15	-	40	80	ns
		PL to Qn; see Figure 4	5	-	135	210	ns
			10	-	78	100	ns
			15	-	72	80	ns
transition time	t _t	Qn; see Figure 4	5	-	60	120	ns
			10	-	30	60	ns
			15	-	20	40	ns
set-up time	t _{su}	DS to CP; see Figure 5	5	+25	+4	-	ns
			10	+25	0	-	ns
			15	+15	0	-	ns
		Dn to PL; see Figure 6	5	50	-11	-	ns
			10	30	-7	-	ns
			15	20	-3	-	ns
hold time	t _h	DS to CP; see Figure 5	5	40	8	-	ns
			10	20	3	-	ns
			15	15	0	-	ns
		Dn to PL; see Figure 6	5	+15	-13	-	ns
			10	15	-9	-	ns
			15	15	-4	-	ns
pulse width	t _w	CP=LOW; minimum width; see Figure 5	5	70	35	-	ns
			10	30	15	-	ns
			15	24	12	-	ns
		PL=HIGH; minimum width; see Figure 6	5	70	35	-	ns
			10	30	15	-	ns
			15	24	12	-	ns
recovery time	t _{rec}	PL input; see Figure 6	5	50	10	-	ns
			10	40	5	-	ns
			15	35	5	-	ns
maximum clock frequency	F _{clk(max)}	CP input; see Figure 5	5	-	13	-	MHz
			10	-	30	-	MHz
			15	-	40	-	MHz



4、Testing Circuit

4.1、AC Testing Circuit



Definitions for test circuit:

DUT=Device Under Test.

C_L =load capacitance including jig and probe capacitance.

R_T =termination resistance should be equal to the output impedance Z_o of the pulse generator.

Figure 3. Test circuit for measuring switching times

4.2、AC Testing Waveforms

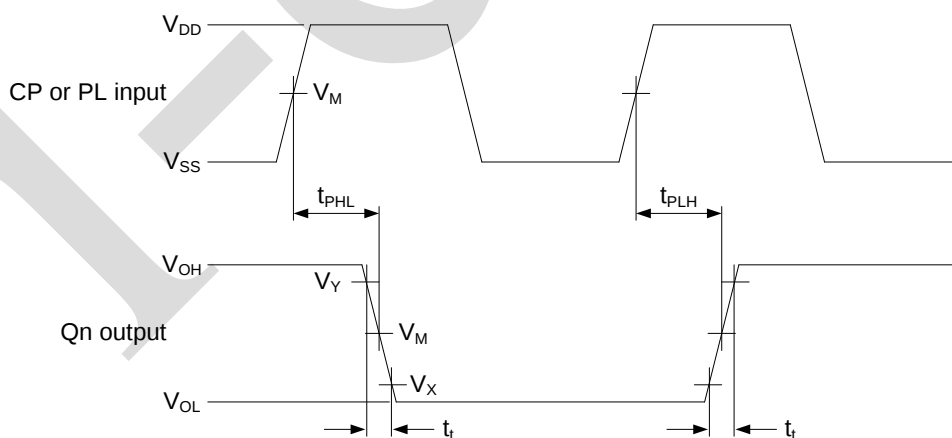


Figure 4. Waveforms showing propagation delays for CP and PL inputs to Qn output and Qn transition times

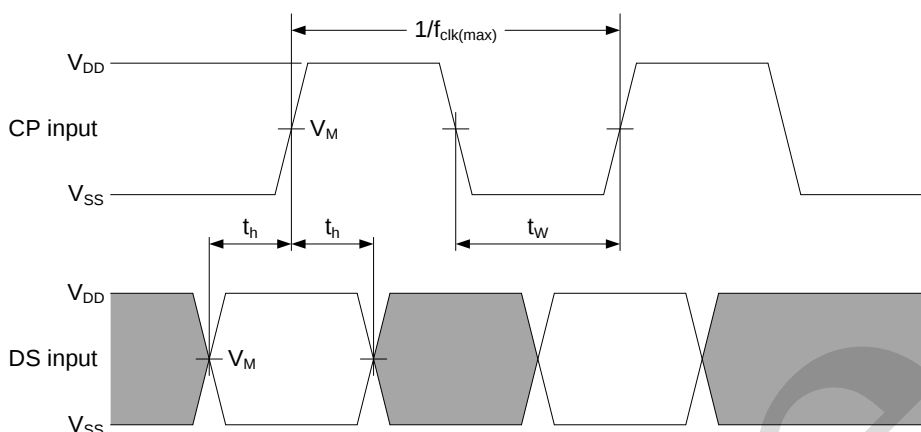


Figure 5. Waveforms showing minimum clock pulse width, set-up time, and hold time for CP and DS.

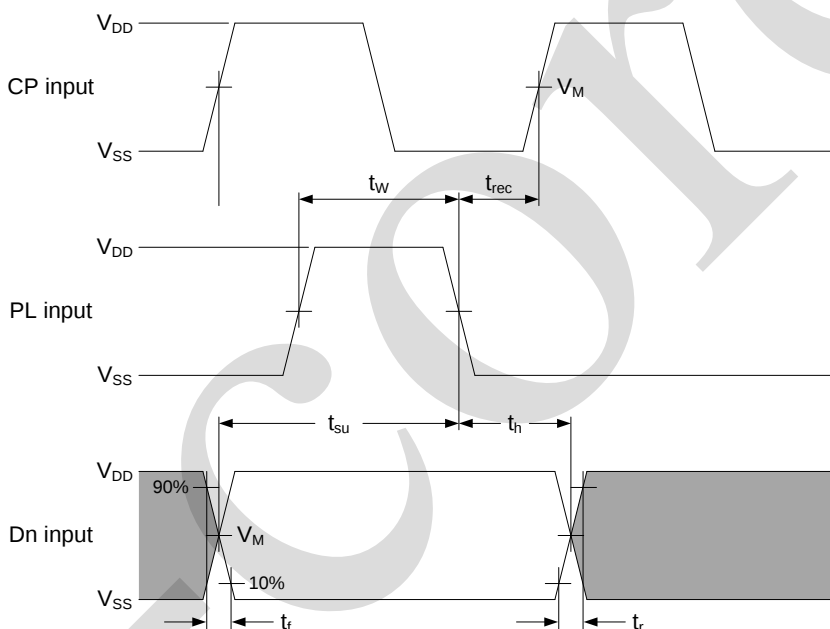


Figure 6. Waveforms showing minimum pulse width and recovery time for PL; set-up and hold times for Dn to PL.

4.3、Measurement Points

Supply voltage	Input	Output		
V_{DD}	V_M	V_M	V_X	V_Y
5V to 15V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$	$0.1 \times V_{DD}$	$0.9 \times V_{DD}$

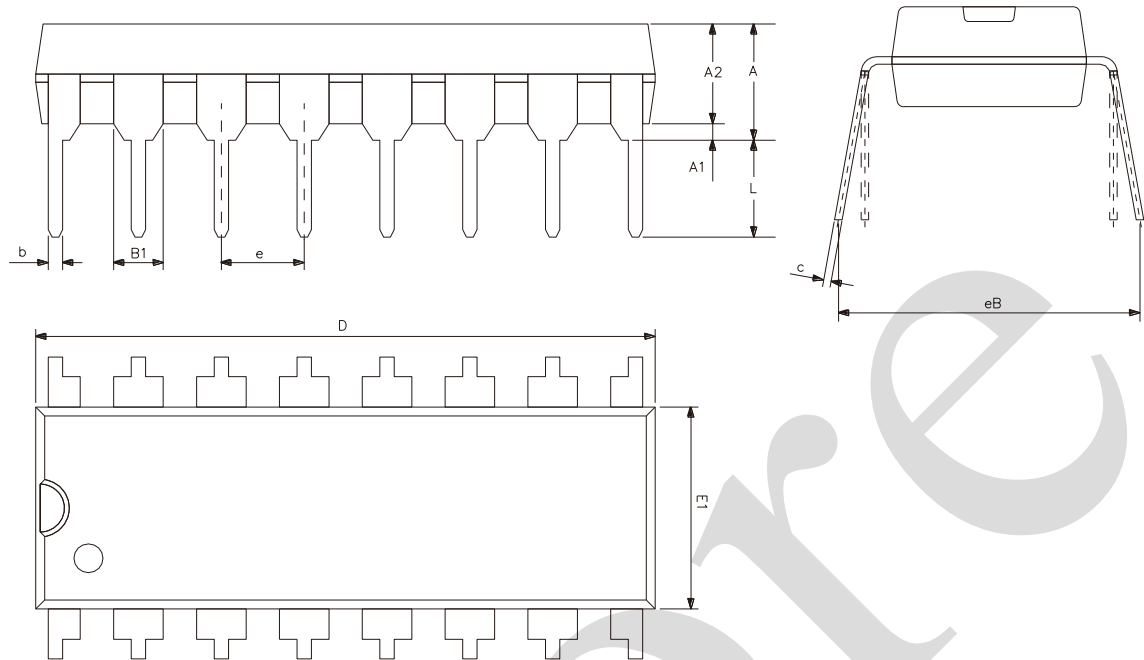
4.4、Test Data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5V to 15V	V_{SS} or V_{DD}	$\leq 20\text{ns}$	50pF



5、Package Information

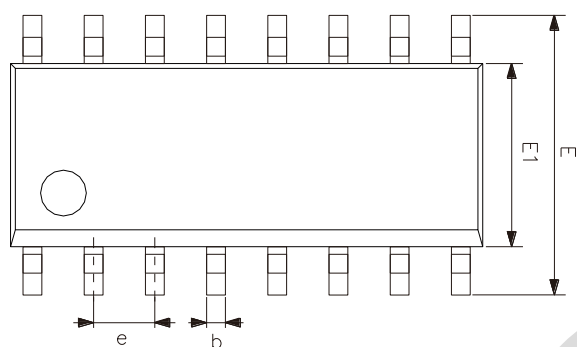
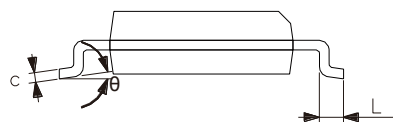
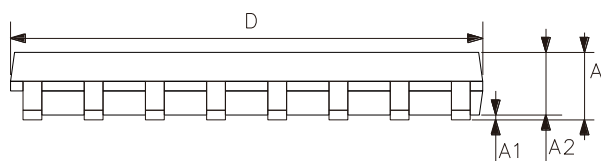
5.1、DIP16



Symbol	Dimensions (mm)	
	Min.	Max.
A2	3.20	3.60
A1	0.51	-
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30



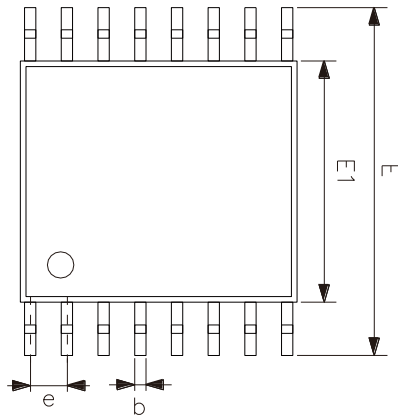
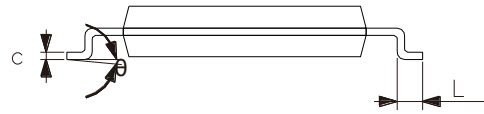
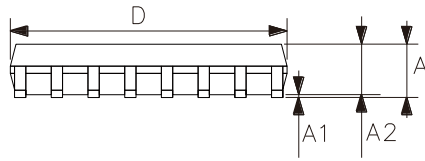
5.2、SOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°



5.3、TSSOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°



6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

We Recommend you to read this chapter carefully before using this product.

The information in this chapter is provided for reference only and i-Core disclaims any express or implied warranties, including but not limited to applicability, special application or non-infringement of third party rights.

This product is not suitable for critical equipment such as life-saving, life-sustaining or safety equipment. It is also not suitable for applications that may result in personal injury, death, or serious property or environmental damage due to product malfunction or failure. I-Core will not be liable for any damages incurred by the customers at their own risk for such applications.

The customer is responsible for conducting all necessary tests i-Core's application to avoid failure in the application or the application of the customer's third party users. I-Core does not accept any liability.

The Company reserves the right to change or improve the information published in this chapter at any time. The information in this chapter are subject to change without notice. We recommend the customer to consult our sales staff before purchasing.

Please obtain related materials from i-Core's regular channels and we are not responsible for its content if it is provided by sources other than our company.

In case of any conflict between the Chinese and English version, the version is subject to the Chinese one.