CD4027
Dual JK Flip-Flop

Product Specification

Specification Revision History:

Version	Date	Description
2019-05-A1	2019-05	New
2023-04-B1	2023-04	Update the template

Contents

1、General Description

The CD4027 is a edge-triggered dual JK flip-flop which features independent set-direct (SD), clear-direct (CD), clock (CP) inputs and outputs (Q, $\overline{Q}$). Data is accepted when CP is LOW, and transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous clear-direct (CD) and set-direct (SD) inputs are independent and override the J, K, and CP inputs. The outputs are buffered for best system performance.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

Features:

- Wide supply voltage range from 3V to 15V
- Fully static operation
- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40℃ to +125℃
- Packaging information: DIP16/SOP16/TSSOP16

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
CD4027DA16.TB	DIP16	CD4027	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
CD4027SA16.TB	SOP16	CD4027	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
CD4027TA16.TB	TSSOP16	CD4027	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
CD4027SA16.TR	SOP16	CD4027	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
CD4027TA16.TR	TSSOP16	CD4027	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

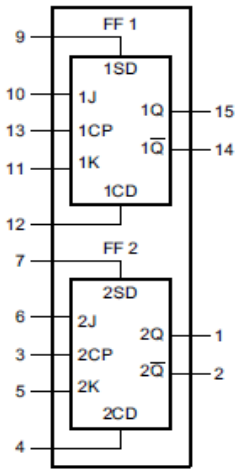


Figure 1. Functional diagram

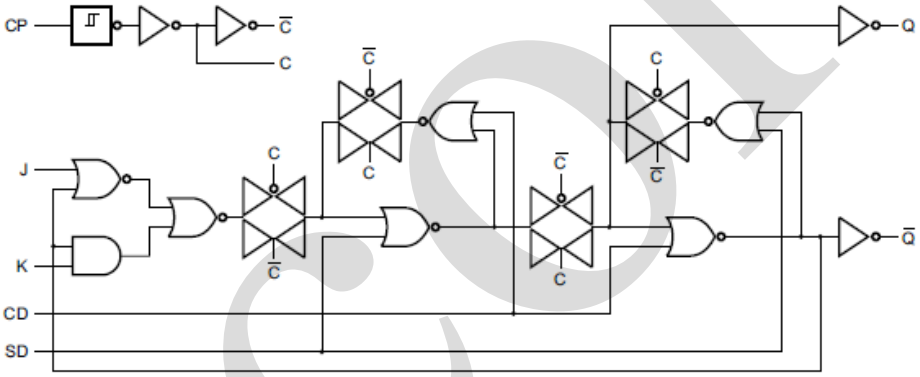
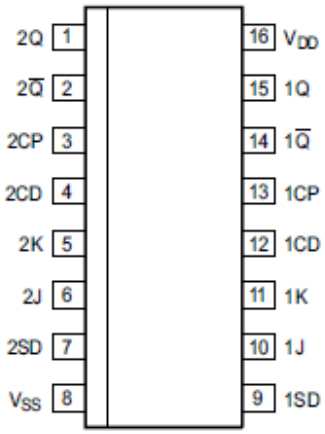


Figure 2. Logic diagram (one flip-flop)

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	2Q	true output
2	$2\bar{Q}$	complement output
3	2CP	clock input (LOW-to-HIGH edge-triggered)
4	2CD	asynchronous clear-direct input (active HIGH)
5	2K	synchronous input
6	2J	synchronous input
7	2SD	asynchronous set-direct input (active HIGH)
8	V_{SS}	ground (0V)
9	1SD	asynchronous set-direct input (active HIGH)
10	1J	synchronous input
11	1K	synchronous input
12	1CD	asynchronous clear-direct input (active HIGH)
13	1CP	clock input (LOW-to-HIGH edge-triggered)
14	$1\bar{Q}$	complement output
15	1Q	true output
16	V_{DD}	supply voltage

2.4、Function Table

Input					Output	
nSD	**nCD**	**nCP**	**nJ**	**nK**	**nQ**	**$n\bar{Q}$**
H	L	X	X	X	H	L
L	H	X	X	X	L	H
H	H	X	X	X	H	H
L	L	↑	L	L	no change	no change
L	L	↑	H	L	H	L
L	L	↑	L	H	L	H
L	L	↑	H	H	$n\bar{Q}$	nQ

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care; ↑=LOW-to-HIGH clock transition.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{DD}	-		-0.5	+18	V
DC input current	I_{IK}	any one input		-	±10	mA
input voltage	V_I	all inputs		-0.5	V_{DD}+0.5	V
storage temperature	T_{stg}	-		-65	+150	℃
total power dissipation	P_{tot}	-		-	500	mW
device dissipation	P	per output transistor		-	100	mW
Soldering temperature	T_L	10s	DIP	245		℃
			SOP/TSSOP	260		℃

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	-	15	V
ambient temperature	T_{amb}	in free air	-40	-	+125	℃
clock pulse width	t_{wCL}	V_{DD}=5V	140	-	-	ns
		V_{DD}=10V	60	-	-	ns
		V_{DD}=15V	40	-	-	ns
clock rise and fall time	t_{rCL}, t_{fCL}	V_{DD}=5V	-	-	45	us
		V_{DD}=10V	-	-	5	us
		V_{DD}=15V	-	-	2	us
clock input frequency	f_{CL}	V_{DD}=5V	DC	-	3.5	MHz
		V_{DD}=10V		-	8	MHz
		V_{DD}=15V		-	12	MHz
set-up time	t_{su}	V_{DD}=5V	200	-	-	ns
		V_{DD}=10V	75	-	-	ns
		V_{DD}=15V	50	-	-	ns
set or reset pulse width	$t_{wS/R}$	V_{DD}=5V	180	-	-	ns
		V_{DD}=10V	80	-	-	ns
		V_{DD}=15V	50	-	-	ns

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)			T_{amb}=25℃			Unit
		V_O	V_{IN}	V_{DD}	Min.	Typ.	Max.	
supply current	I_{DD}	-	0, 5	5	-	-	1	uA
		-	0, 10	10	-	-	2	uA
		-	0, 15	15	-	-	4	uA
LOW-level output current	I_{OL}	0.4	0, 5	5	0.51	1	-	mA
		0.5	0, 10	10	1.3	2.6	-	mA
		1.5	0, 15	15	3.4	6.8	-	mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-0.51	-1	-	mA
		2.5	0, 5	5	-1.6	-3.2	-	mA
		9.5	0, 10	10	-1.3	-2.6	-	mA
		13.5	0, 15	15	-3.4	-6.8	-	mA
LOW-level output voltage	V_{OL}	-	0, 5	5	-	0	0.05	V
		-	0, 10	10	-	0	0.05	V
		-	0, 15	15	-	0	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	5	-	V
		-	0, 10	10	9.95	10	-	V
		-	0, 15	15	14.95	15	-	V
LOW-level input voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	V
		1, 9	-	10	-	-	3	V
		1.5, 13.5	-	15	-	-	4	V
HIGH-level input voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	V
		1, 9	-	10	7	-	-	V
		1.5, 13.5	-	15	11	-	-	V
input leakage current	I_I	-	0, 15	15	-	-	±1	uA

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)			T_{amb}=-40℃		T_{amb}=+85℃		T_{amb}=+125℃		Unit
		V_O	V_{IN}	V_{DD}	Min.	Max.	Min.	Max.	Min.	Max.	
supply current	I_{DD}	-	0, 5	5	-	1	-	30	-	30	uA
		-	0, 10	10	-	2	-	60	-	60	uA
		-	0, 15	15	-	4	-	120	-	120	uA
LOW-level output current	I_{OL}	0.4	0, 5	5	0.61	-	0.42	-	0.36	-	mA
		0.5	0, 10	10	1.5	-	1.1	-	0.9	-	mA
		1.5	0, 15	15	4	-	2.8	-	2.4	-	mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-0.61	-	-0.42	-	-0.36	-	mA
		2.5	0, 5	5	-1.8	-	-1.3	-	-1.15	-	mA
		9.5	0, 10	10	-1.5	-	-1.1	-	-0.9	-	mA
		13.5	0, 15	15	-4	-	-2.8	-	-2.4	-	mA
LOW-level output voltage	V_{OL}	-	0, 5	5	-	0.05	-	0.05	-	0.05	V
		-	0, 10	10	-	0.05	-	0.05	-	0.05	V
		-	0, 15	15	-	0.05	-	0.05	-	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	-	4.95	-	4.95	-	V
		-	0, 10	10	9.95	-	9.95	-	9.95	-	V
		-	0, 15	15	14.95	-	14.95	-	14.95	-	V
LOW-level input voltage	V_{IL}	0.5, 4.5	-	5	-	1.5	-	1.5	-	1.5	V
		1, 9	-	10	-	3	-	3	-	3	V
		1.5, 13.5	-	15	-	4	-	4	-	4	V
HIGH-level input voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	7	-	V
		1.5, 13.5	-	15	11	-	11	-	11	-	V
input leakage current	I_I	-	0, 15	15	-	±1	-	±1	-	±1	uA

3.3.3、AC Characteristics

(T_{amb}=25℃, V_{SS}=0V, t_r, t_f=20ns, C_L=50pF, R_L=200kΩ, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH to LOW propagation delay	t_{PHL}	nCP to nQ, $n\overline{Q}$; see Figure 4	V_{DD}=5V	-	150	300	ns
			V_{DD}=10V	-	65	130	ns
			V_{DD}=15V	-	45	90	ns
		nSD to $n\overline{Q}$ or nCD to nQ see Figure 4	V_{DD}=5V	-	200	400	ns
			V_{DD}=10V	-	85	170	ns
			V_{DD}=15V	-	60	120	ns
LOW to HIGH propagation delay	t_{PLH}	nCP to nQ, $n\overline{Q}$; see Figure 4	V_{DD}=5V	-	150	300	ns
			V_{DD}=10V	-	65	130	ns
			V_{DD}=15V	-	45	90	ns
		nSD to nQ or nCD to $n\overline{Q}$ see Figure 4	V_{DD}=5V	-	150	300	ns
			V_{DD}=10V	-	65	130	ns
			V_{DD}=15V	-	45	90	ns
transition time	t_t	see Figure 4	V_{DD}=5V	-	100	200	ns
			V_{DD}=10V	-	50	100	ns
			V_{DD}=15V	-	40	80	ns
maximum clock frequency	$f_{clk(max)}$	nCP input; nJ=nK=HIGH; see Figure 5	V_{DD}=5V	3.5	7	-	MHz
			V_{DD}=10V	8	16	-	MHz
			V_{DD}=15V	12	24	-	MHz
pulse width	t_W	nCP LOW; minimum width see Figure 5	V_{DD}=5V	-	70	140	ns
			V_{DD}=10V	-	30	60	ns
			V_{DD}=15V	-	20	40	ns
		nSD, nCD HIGH; minimum width see Figure 6	V_{DD}=5V	-	90	180	ns
			V_{DD}=10V	-	40	80	ns
			V_{DD}=15V	-	25	50	ns
set-up time	t_{su}	nJ, nK to nCP; see Figure 5	V_{DD}=5V	-	100	200	ns
			V_{DD}=10V	-	35	75	ns
			V_{DD}=15V	-	25	50	ns
clock input rise and fall time	t_{rCL}, t_{fCL}	-	V_{DD}=5V	-	-	45	us
			V_{DD}=10V	-	-	5	us
			V_{DD}=15V	-	-	2	us
input capacitance	C_I	any input		-	5	7.5	pF

Note: t_t is the same as t_{TLH} and t_{THL}.

4、Testing Circuit

4.1、AC Testing Circuit

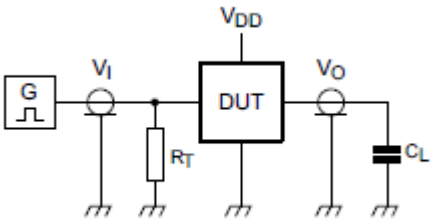


Figure 3. Test circuit for switching times

Definitions for test circuit:
DUT=Device Under Test.
C_L=Load capacitance including jig and probe capacitance.
R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

4.2、AC Testing Waveforms

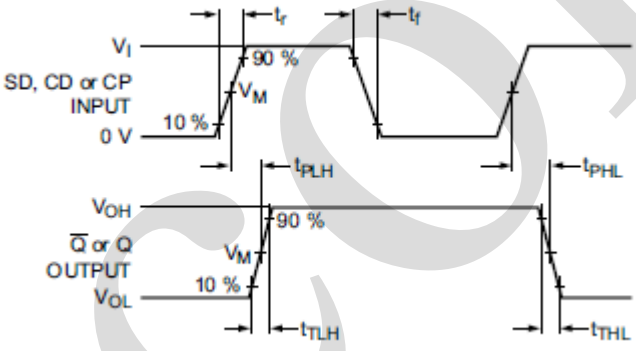


Figure 4. Waveforms showing rise, fall and transition times and propagation delays

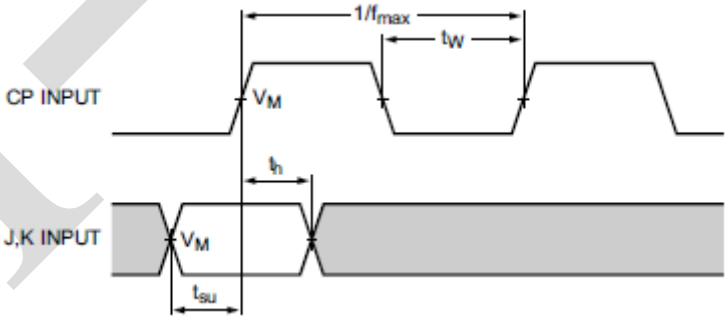


Figure 5. Waveforms showing set-up and hold times and minimum clock pulse width

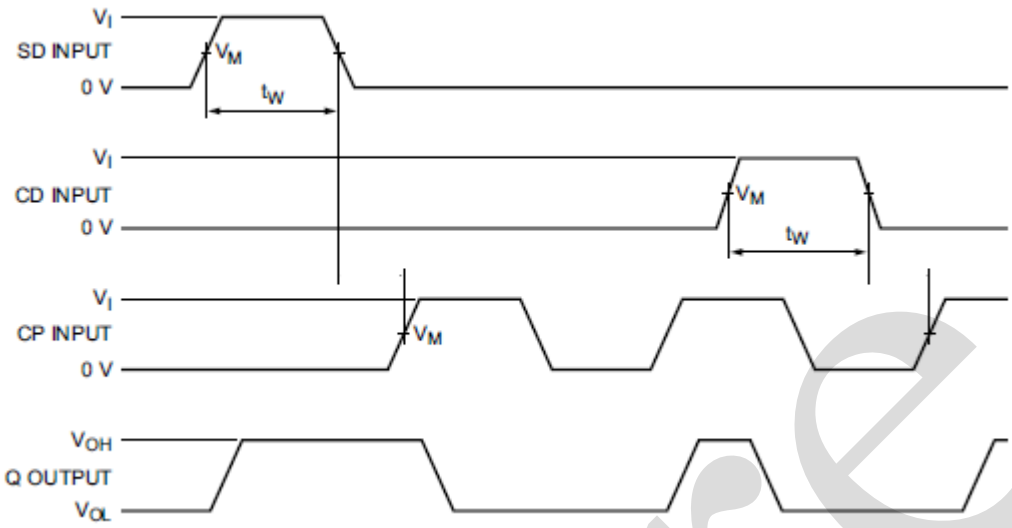


Figure 6. Waveforms showing pulse widths

4.3、Measurement points

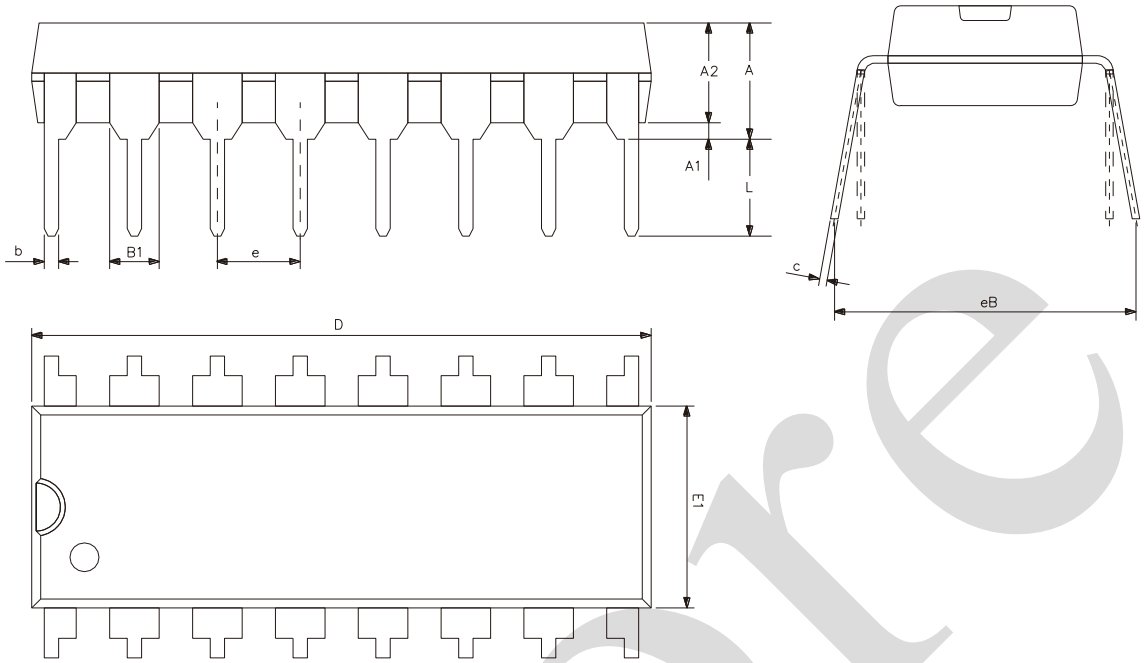
Supply voltage	Input	Output
V_{DD}	V_M	V_M
5V to 15V	$0.5\times V_{DD}$	$0.5\times V_{DD}$

4.4、Test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r , t_f	C_L
5V to 15V	V_{SS} or V_{DD}	≤ 20ns	50pF

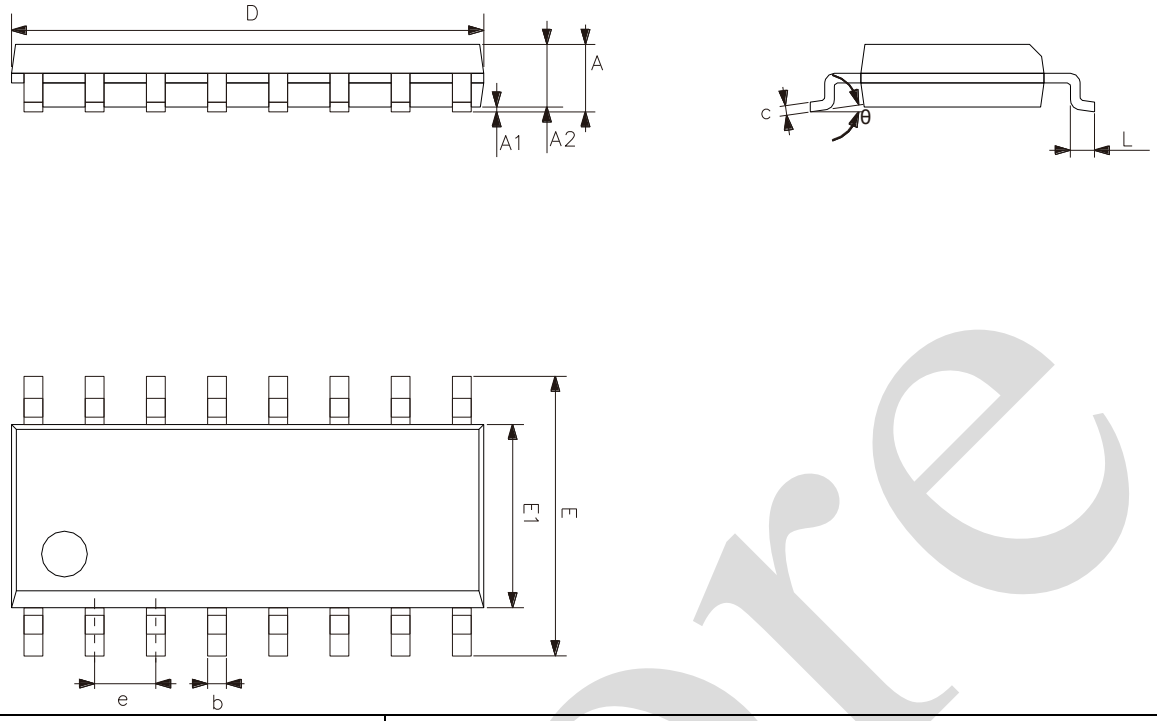
5、Package Information

5.1、DIP16



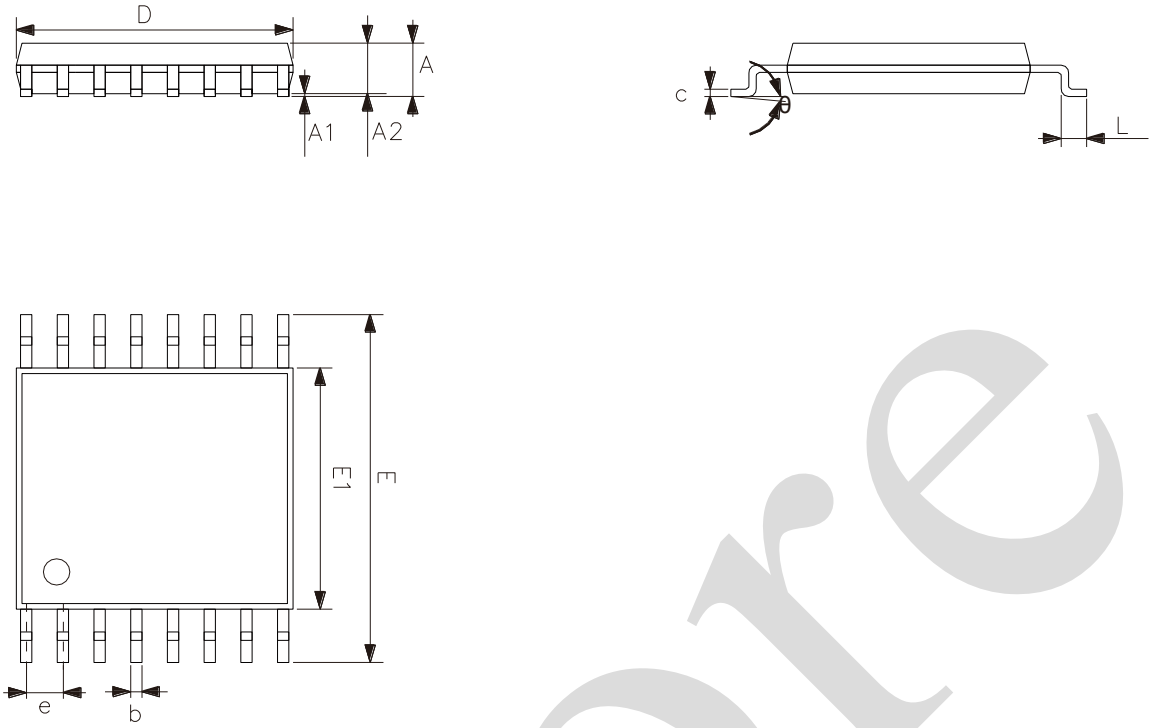
Symbol	Dimensions (mm)	
	Min.	Max.
A2	3.20	3.60
A1	0.51	-
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30

5.2、SOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°

5.3、TSSOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

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