Pulse width modulation circuit UC3844A

Overview and characteristics

UC 3844A Is the pulse width modulation integrated circuit with the current control mode of the switching power supply. Compared with the voltage control mode, it has many advantages in the aspects of load response and linear adjustment. Have SOP8, DIP 8 package form.

The main features of the circuit are:

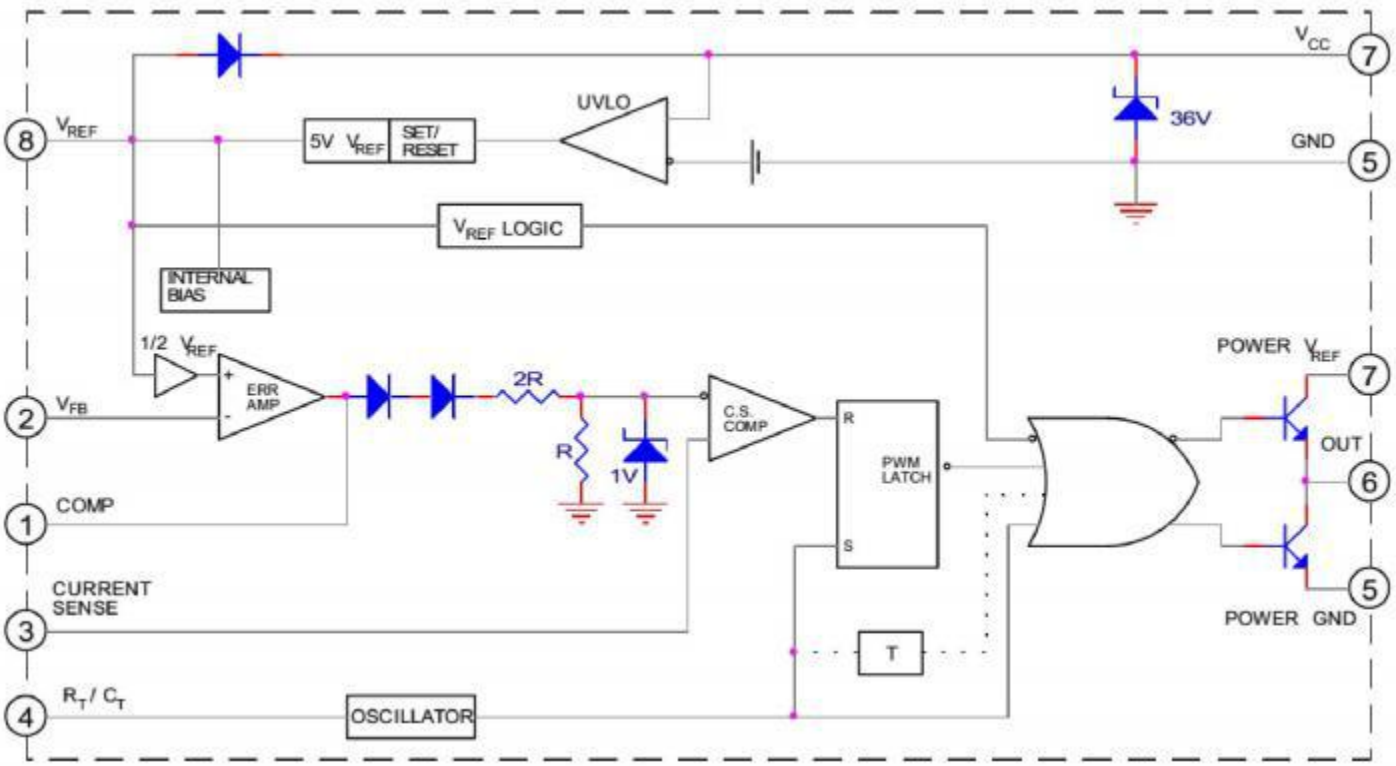
- Contains an undervoltage locking circuit
- Low start current (typical value is 0.12mA)
- Stable internal reference voltage source
- High current push-pull output (drive current up to 1A)
- Operating frequency is up to 500kHz
- Automatic negative feedback compensation circuit
- Double pulse inhibition
- Strong load-response characteristics

Packaging form:

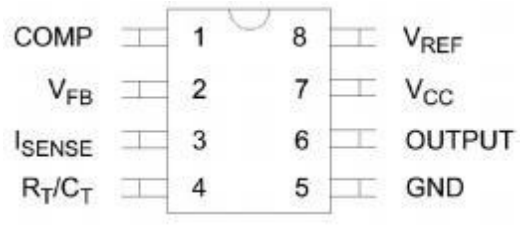
SOIC -8

DIP -8

block diagram



Lead-end function



order number	symbol	function	order number	symbol	function
1	C OMP	Compare the end	5	GND	the earth
2	VFB	degenerative feedback	6	OUTPU T	output
3	ISENSE	current sensitivity	7	V CC	source
4	RT/CT	Oscillation end	8	VREF	reference voltage

Maximum rating (Tamb = 25℃, unless otherwise noted)

The parameter name	symbol	numeric value	unit
supply voltage	V cc	30	V
output	Io	±1	A
Error amplifier current	Isink (EA)	10	m A
Error amplifier input voltage	Vin (EA)	-0.3~+6.3	V
power dissipation	PD (DIP)	1	W
operating ambient temperature	T amb	0~70	℃
Storage temperature	T stg	-55~150	℃

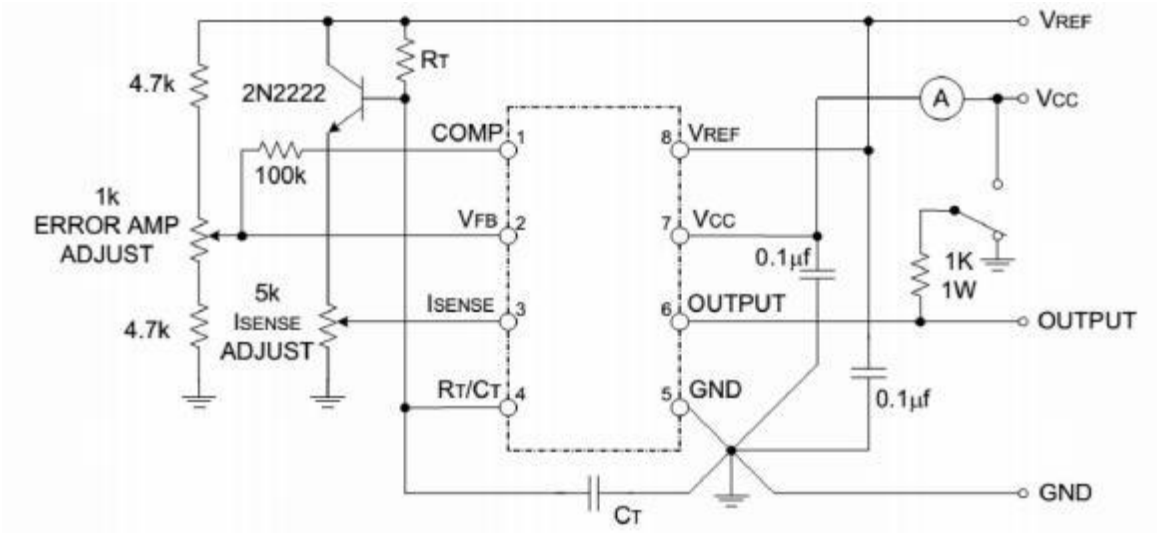
Electrical characteristics (Vcc =15V, RT=10k Ω, CT=3.3nF , Tamb =0℃~70℃)

The parameter name	symbol	test condition	mini mum	typical case	maxi mum	unit
Reference electricity, source part						
reference voltage	VREF	Tj =25C, IREF=1mA	4.90	5.00	5.10	V
Linear adjustment rate	Δ VREF	12V ≤Vcc≤25V		6	20	m V
load regulation	Δ VREF	1mA ≤ IREF20mA		6	25	m V
Short-circuit transmission,	Isc	Tamb =25℃	-30	-100	-180	m A

and current output						
oscillating part						
oscillation frequency	f_{OSC}	Tj =25℃	47	52	57	kHz
Frequency and voltage characteristics	Δ f /Δ VCC	12V ≤Vcc≤25V		0.05	1	%
oscillation amplitude	V(OSC)	4 Foot peak peak value		1.6		Vp p
Error amplifier part (EA)						
input bias current	IBIAS			-0.1	-2	μA
input voltage	Vin(EA)	V1=2.5V	2.42	2.50	2.58	V
open loop voltage gain	GV O	2V≤VO≤4V	60	90		d B
Current inhibition ratio	P SRR	12V ≤VCC≤25V	60	70		d B
Output irrigation current	ISINK	V2=2.7V, V1=1.1V	2	6		m A
Output suction current	ISOURCE	V2=2.3V, V1=5V	-0.5	-0.8		m A
Output high level	VO H	V2=2.3V , RL=15kΩ to GND	5	6		V
output low level	VOL	V2=2.7V , RL=15kΩ to Pin8		0.7	1.1	V

Current sensitivity part						
gain	GV		2.85	3	3.15	V/V
maximum input signal	$V_{I\ (MAX)}$	V1=5V	0.9	1	1.1	V
power supply rejection ratio	P SRR	12V ≤VCC≤25V		70		d B
input bias current	IBIAS			-2	-10	μA
output part						
output low level	V OL	ISINK=20m A		0.1	0.4	V
		ISINK=200mA		1.5	2.2	V
Output high level	VO H	ISOURCE=20mA	13	13.5		V
		ISOURCE=200mA	12	13.0		V
rise time	tr	CL=1nF		50	150	n s
drop-out time	t f	CL=1nF		50	150	n s
UVL circuit						
Start valve value	$V_{TH\ (ST)}$		14.5	16.0	17.5	V
Minimum operating voltage	$V_{OPR\ (MIN)}$		8.5	10.0	11.5	V
PWM part						
Maximum duty cycle	D(MAX)		47	48	50	%
Minimum duty cycle	D(MIN)				0	%
current						
starting current	IS T			0.12	0.3	m A
Action power supply current	$I_{CC\ (OPR)}$	V3=V2=0V		11	17	m A
Zener voltage	VZ	Icc=25mA		34		V

Basic test circuit


VREF
RT
4.7k
2N2222
A
VCC
COMP 1
8 VREF
100k
1k
ERROR AMP
ADJUST
VFB 2
7 VCC
0.1µf
1K
1W
5k
ISENSE
ADJUST
ISENSE 3
6 OUTPUT
OUTPUT
4.7k
RT/CT 4
5 GND
0.1µf
GND
CT