# 24-bit Sigma-Delta ADC with Gain=64 Ultra-Low-Noise Amplifier

## FEATURES

**Amplifier Gain: 64**
**Selectable Data Rates: 1.875 to 3840SPS**
**RMS Noise: 16nV at 7.5SPS**
**20.4 Noise-Free Bits at 1.875SPS**
**Offset Drift: 5nV/°C**
**Gain Drift: 0.5ppm/°C**
**Integral Non-Linearity: 3ppm**
**Internal or External Clock**
**Burnout Current Sources**
**Parity Check**
**Power Supply**
- **AVDD: 4.75V to 5.25V or ±2.5V**
- **DVDD: 2.7V to 5.25V**

**Current: 4.0mA**
**Package: 20-lead TSSOP**

## APPLICATIONS

**Weigh Scales**
**Strain Gauges**
**Pressure Sensors**
**Industrial Process Control**

## DESCRIPTION

The SIG5530 is a low noise, low drift, and high-resolution 24-bit analog-to-digital converter (ADC) with integrated gain amplifier that offers high-accuracy measurement solutions for bridge sensors.

The device contains an ultra-low-noise amplifier with fixed gain 64, a delta-sigma (Δ-Σ) modulator, and a programmable SINC3/SINC1 digital filter. The output data rate from the device can be configured to 1.875, 3.75, 7.5, 15, 30, 60, 120, 240, 480, 960, 1920, and 3840SPS. Burnout current sources are provided at the analog inputs for sensor connection diagnosis.

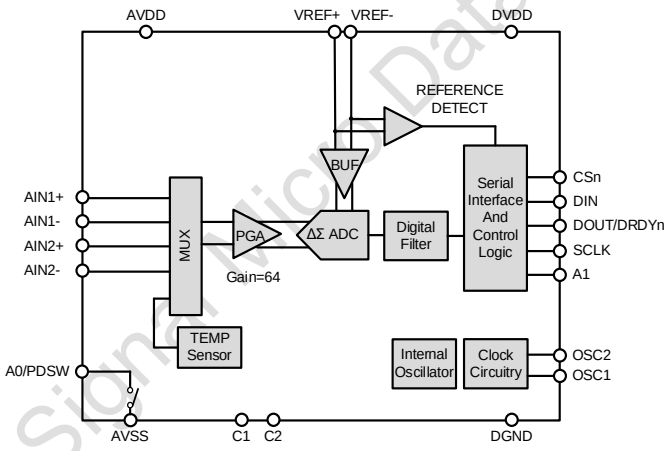
Offset and gain calibration registers are provided with calibration command or direct register write to calibrate the ADC errors or overall system errors. SPI-compatible interface is used for device configuration and parity check is provided for data integrity.

The on-chip oscillator, an external clock, or an external crystal can be used as the clock source to the device.

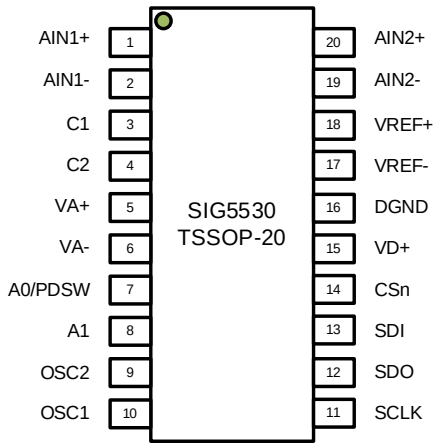
The device can operate with bipolar ±2.375V to ±2.625V analog power supplies, or with a single 4.75V to 5.25V analog power supply.

The SIG5530 is available in 20-lead TSSOP package. These devices are fully specified over the -40°C to +125°C temperature range.

### Function Block Diagram

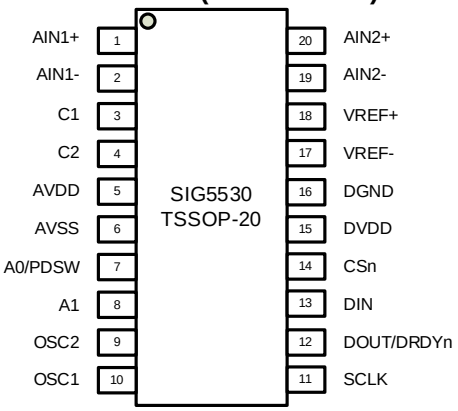



### TSSOP-20



# PIN CONFIGURATION and DESCRIPTIONS

**TOP VIEW (Not To Scale)**




| PIN | | FUNCTION | DESCRIPTION |
|---|---|---|---|
| No. | NAME | | |
| 1 | AIN1+ | Analog Input | Positive analog input channel 1. |
| 2 | AIN1- | Analog Input | Negative analog input channel 1. |
| 3 | C1 | Analog Output | Amplifier analog output. Connect a COG cap with size 4.7~22nF between C1 and C2. |
| 4 | C2 | Analog Output | Amplifier analog output. Connect a COG cap with size 4.7~22nF between C1 and C2. |
| 5 | AVDD | Analog | Positive analog power supply. 4.75V to 5.25V relative to AVSS. |
| 6 | AVSS | Analog | Negative analog power supply. |
| 7 | A0/PDSW | Analog Output | Analog logic output or bridge power down switch. |
| 8 | A1 | Analog Output | Analog logic output. |
| 9 | OSC2 | Digital Input/Output | Master clock input or Crystal Connection. |
| 10 | OSC1 | Digital Input | Crystal Connection. |
| 11 | SCLK | Digital Input | Serial data clock. |
| 12 | DOUT/DRDYn | Digital Output | Serial data output and data ready indicator. |
| 13 | DIN | Digital Input | Serial data input. |
| 14 | CSn | Digital Input | Serial chip select. Active low. |
| 15 | DVDD | Digital | Digital power supply, 2.7V to 5.25V. DVDD is independent of AVDD. |
| 16 | DGND | Digital | Digital ground reference point. |
| 17 | REF- | Analog Input | Negative reference input. |
| 18 | REF+ | Analog Input | Positive reference input. |
| 19 | AIN2- | Analog Input | Negative analog input channel 2. |
| 20 | AIN2+ | Analog Input | Positive analog input channel 2. |

# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKING OPTION |
|---|---|---|---|---|
| SIG5530 | TSSOP-20 | -40°C to +125°C | SIG5530-ITSP20-RL | Reel, 4500 |

# SPECIFICATIONS

## Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | AVDD to AVSS | –0.3 | 6.5 | V |
| | AVSS to DGND | –3 | 0.3 | V |
| | DVDD to DGND | –0.3 | 6.5 | V |
| | Analog input | $V_{AVSS}$ – 0.3 | $V_{AVDD}$ + 0.3 | V |
| | Digital input | $V_{DGND}$ – 0.3 | $V_{DVDD}$ + 0.3 | V |
| Current | Input current | –10 | 10 | mA |
| Temperature | Junction ($T_J$) | –50 | 150 | °C |
| | Storage ($T_{stg}$) | -60 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD Ratings

| SYMBOL | PARAMTER | CONDITION | VALUE | UNIT |
|---|---|---|---|---|
| HBM | Human-body Model | ANSI/ESDA/JEDEC JS-001 | ±4000 | V |
| CDM | Charged-device model | JEDEC EIA/JS-002-2022 | ±2000 | V |

This integrated circuit can be damaged by ESD. Signal Micro recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## Electrical Characteristics

Minimum/Maximum specifications apply from -40˚C to +125˚C. Typical specifications are at +25˚C. All specification are at $V_{AVDD}$=5V, $V_{AVSS}$=0V, $V_{DVDD}$=3.3V, $V_{REF}$=2.5V, $f_{CLK}$=4.9152MHz, data rate=60SPS, unless otherwise noted.

| PARAMETER | TEST CONDITION OR NOTES | MIN(1) | TYP | MAX(1) | UNITS |
|---|---|---|---|---|---|
| **ANALOG INPUTS** | | | | | |
| Differential Input Voltage | $V_{IN} = V_{INP} – V_{INN}$ | $–V_{REF}/(2xGain)$ | | $+V_{REF}/(2xGain)$ | V |
| Absolute Input Voltage | | $V_{AVSS}$ + 0.5 | | $V_{AVDD}$ – 0.5 | V |
| Common Mode Input Range | GAIN=64 | $V_{AVSS}$ + 0.5 + $\lvert V_{INMAX}\rvert \cdot 32$ | | $V_{AVDD}$ – 0.5 – $\lvert V_{INMAX}\rvert \cdot 32$ | V |
| Absolute Input Current | | | ±2 | | nA |
| **SYSTEM PERFORMANCE** | | | | | |
| Amplifier Gain | | | 64 | | V/V |
| Resolution | | | 24 | | Bits |
| Data Rate | | 1.875 | | 3840 | SPS |
| Noise | | | See Noise Table | | |
| Integral Nonlinearity (INL) | | | ±3 | | ppm |
| Offset Error | | | ±3 | | µV |
| Offset Drift vs. Temperature | | | ± 5 | | nV/°C |
| Gain Error(2) | | -350 | ±100 | 350 | ppm |
| Gain Drift vs. Temperature | | -3 | ±0.5 | 3 | ppm/°C |
| Common Mode Rejection (CMRR) | $f_{IN}$=50/60Hz, data rate=960SPS | 100 | 120 | | dB |
| Power Supply Rejection (PSRR) | AVDD, AVSS | 75 | 90 | | dB |
| | DVDD | 80 | 120 | | dB |
| **REFERENCE INPUT** | | | | | |
| Differential Reference Voltage ($V_{REF}$) | $V_{REF} = V_{REFP} – V_{REFN}$ | 0.5 | | $V_{AVDD} – V_{AVSS}$ + 0.1 | V |
| Absolute Negative Reference Voltage ($V_{REFN}$) | | $V_{AVSS}$ – 0.05 | | $V_{REFP}$ – 0.5 | V |
| Absolute Positive Reference Voltage ($V_{REFP}$) | | $V_{REFN}$ + 0.5 | | $V_{AVDD}$ + 0.05 | V |
| Average Voltage Input Current | | | 300 | | nA |
| **Burnout Current Sources** | | | | | |
| Current Setting | | | 1 | | µA |
| **ADC CLOCK** | | | | | |
| External Clock | Frequency Range | 1 | 4.9152 | 5 | MHz |
| | Duty Cycle | 40% | | 60% | |
| Internal Oscillator | Nominal Frequency | | 4.9152 | | MHz |
| | Accuracy | –3% | ±0.5% | 3% | |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| High-level Output Voltage ($V_{OH}$) | $I_{OH}$ = 4mA | $0.8 \cdot V_{DVDD}$ | | | V |
| Low-level Output Voltage ($V_{OL}$) | $I_{OL}$ = –4mA | | | $0.2 \cdot V_{DVDD}$ | V |
| High-level Input Voltage ($V_{IH}$) | | $0.7 \cdot V_{DVDD}$ | | $V_{DVDD}$ | V |
| Low-level Input Voltage ($V_{IL}$) | | $V_{DGND}$ | | $0.3 \cdot V_{DVDD}$ | V |
| Input Hysteresis | | | 0.5 | | V |
| Input Leakage | | | | ±10 | µA |
| **POWER SUPPLY** | | | | | |
| AVSS Voltage ($V_{AVSS}$) | | –2.625 | | 0 | V |
| AVDD Voltage ($V_{AVDD}$) | | $V_{AVSS}$ + 4.75 | | $V_{AVSS}$ + 5.25 | V |
| DVDD Voltage ($V_{DVDD}$) | | 2.7 | | 5.25 | V |
| AVDD, AVSS Current ($I_{AVDD}$) | Active Mode | | 3.6 | 4.5 | mA |
| | Sleep Mode | | 1 | | µA |

| | | | | | |
|---|---|---|---|---|---|
| DVDD Current ($I_{DVDD}$) | Active Mode | | 0.4 | 0.6 | mA |
| | Sleep Mode | | 40 | | µA |
| Total Power Dissipation | Active Mode | | 20 | | mW |
| | Sleep Mode | | 0.15 | | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified temperature range | | –40 | | 125 | °C |
| Operating temperature range | | –50 | | 125 | °C |
| Storage temperature range | | –60 | | 150 | °C |

(1) Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
(2) MIN and MAX values listed for gain error are for +25˚C room temperature only.

## Timing Requirements: Serial Interface

Over the operating ambient temperature range and DVDD = 2.7V to 5.25V, unless otherwise noted.

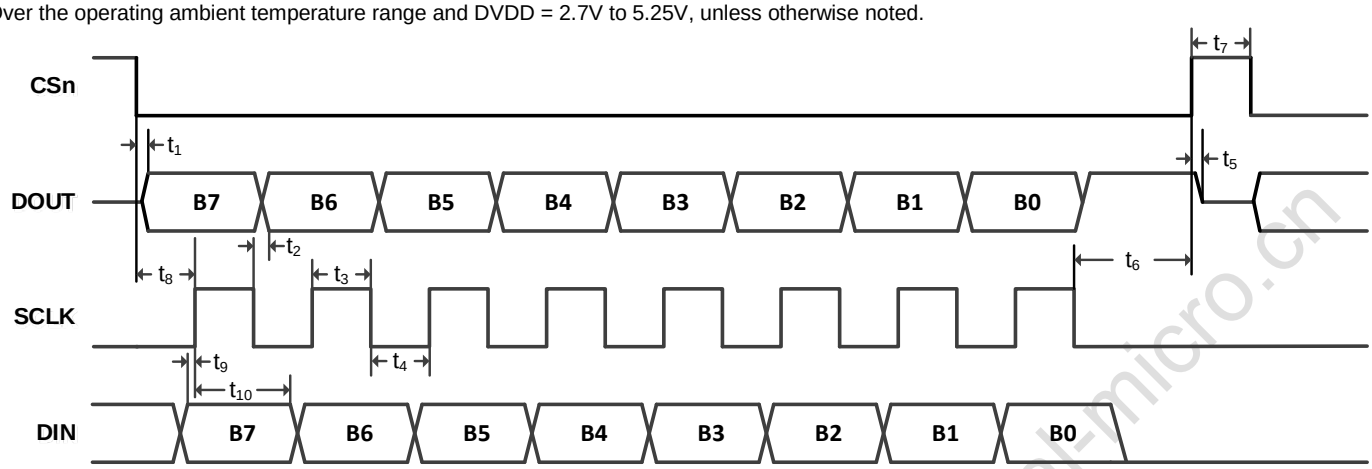



**Figure 1. Serial Interface Timing Requirements**

| SYMBOL | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_1$ | CSn falling edge to valid DOUT/DRDYn: propagation delay(1) | | 20 | ns |
| $t_2$ | SCLK falling edge to valid DOUT/DRDYn: propagation delay(1) | | 20 | ns |
| $t_3$ | SCLK high pulse width | 50 | | ns |
| $t_4$ | SCLK low pulse width | 50 | | ns |
| | SCLK period | 100 | $10^6$ | ns |
| $t_5$ | CSn rising edge to DOUT high impedance: propagation delay | | 20 | ns |
| $t_6$ | Last SCLK falling edge to CSn rising edge: delay time | 20 | | ns |
| $t_7$ | CSn high pulse width | 50 | | ns |
| $t_8$ | CSn falling edge to first SCLK rising edge: setup time(2) | 50 | | ns |
| $t_9$ | Valid DIN to SCLK rising edge: setup time | 20 | | ns |
| $t_{10}$ | Valid DIN to SCLK rising edge: hold time | 20 | | ns |

(1) DOUT load = 20pF || 100kΩ to DGND.
(2) CSn can be tied low.

## NOISE PERFORMANCE

The noise performance of the ADC is affected by amplifier gain, data rate, and digital filter setting. The following tables show the rms noise and peak-to-peak noise for SINC3 and SINC1 filters. The effective number of bits (ENOB) and noise-free bits are also listed according to Equation (1) and Equation (2):

$$\text{ENOB} = \log_2(2 \times V_{REF} / \text{Gain} / V_{RMS}) \quad (1)$$

$$\text{Noise Free Bits} = \log_2(2 \times V_{REF} / \text{Gain} / V_{p\text{-}p}) \quad (2)$$

The noise data listed in the table are typical and are generated from continuous ADC readings with differential input voltage of 0 V.

**Table 1. ADC Noise in μVRMS (μVPP) at $T_A$ = 25°C, $V_{AVDD}$ = 5 V, $V_{AVSS}$ = 0 V, $V_{REF}$ = 2.5 V, SINC3 Filter**

| Data Rate(SPS) | GAIN=64 |
|---|---|
| 1.875 | 0.008(0.050) |
| 3.75 | 0.011(0.070) |
| 7.5 | 0.016(0.099) |
| 15 | 0.023(0.140) |
| 30 | 0.032(0.198) |
| 60 | 0.045(0.280) |
| 120 | 0.064(0.396) |
| 240 | 0.091(0.561) |
| 480 | 0.128(0.793) |
| 960 | 0.182(1.12) |
| 1920 | 0.255(1.55) |
| 3840 | 0.357(2.47) |

**Table 2. ADC ENOB (Noise Free Bits) at $T_A$ = 25°C, $V_{AVDD}$ = 5 V, $V_{AVSS}$ = 0 V, $V_{REF}$ = 5 V, SINC3 Filter**

| Data Rate(SPS) | GAIN=64 |
|---|---|
| 1.875 | 23.2(20.4) |
| 3.75 | 22.7(19.9) |
| 7.5 | 22.2(19.4) |
| 15 | 21.7(18.9) |
| 30 | 21.2(18.4) |
| 60 | 20.7(17.9) |
| 120 | 20.2(17.4) |
| 240 | 19.7(16.9) |
| 480 | 19.2(16.4) |
| 960 | 18.7(15.9) |
| 1920 | 18.2(15.3) |
| 3840 | 17.7(14.9) |

**Table 3. ADC Noise in μVRMS (μVPP) at $T_A$ = 25°C, $V_{AVDD}$ = 5 V, $V_{AVSS}$ = 0 V, $V_{REF}$ = 2.5 V, SINC1 Filter**

| Data Rate(SPS) | GAIN=64 |
|---|---|
| 1.875 | 0.010(0.062) |
| 3.75 | 0.014(0.088) |
| 7.5 | 0.020(0.125) |
| 15 | 0.029(0.176) |
| 30 | 0.041(0.249) |
| 60 | 0.057(0.352) |
| 120 | 0.081(0.498) |
| 240 | 0.115(0.705) |
| 480 | 0.163(0.996) |
| 960 | 0.230(1.41) |
| 1920 | 0.317(2.20) |
| 3840 | 0.397(3.00) |

**Table 4. ADC ENOB (Noise Free Bits) at $T_A$ = 25°C, $V_{AVDD}$ = 5 V, $V_{AVSS}$ = 0 V, $V_{REF}$ = 5 V, SINC1 Filter**

| Data Rate(SPS) | GAIN=64 |
|---|---|
| 1.875 | 22.8(20.1) |
| 3.75 | 22.3(19.6) |
| 7.5 | 21.8(19.1) |
| 15 | 21.3(18.6) |
| 30 | 20.8(18.1) |
| 60 | 20.3(17.6) |
| 120 | 19.8(17.1) |
| 240 | 19.3(16.6) |
| 480 | 18.8(16.1) |
| 960 | 18.3(15.6) |
| 1920 | 17.9(15.0) |
| 3840 | 17.5(14.9) |

# REGISTER MAPS

There are total three 32-bit registers inside the device. These registers are used to configure and control the ADC to the desired mode of operation. These registers can be accessed through the SPI-compatible serial interface by using register read and write commands. At power-on or reset, the registers default to their initial settings, as shown in the *Reset Value* column of Table 5.

**Table 5. Register map**

| ADDR. RS[2:0] | NAME | RESET VALUE | BIT 31 | BIT 30 | BIT 29 | BIT 28 | BIT 27 | BIT26 | BIT 25 | BIT 24 |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | BIT 23 | BIT 22 | BIT 21 | BIT 20 | BIT 19 | BIT18 | BIT 17 | BIT 16 |
| | | | BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT10 | BIT 9 | BIT 8 |
| | | | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| 3'b001 | OFFSET | 0x00000000 | OFFSET[31:24] | | | | | | | |
| | | | OFFSET[23:16] | | | | | | | |
| | | | OFFSET[15:8] | | | | | | | |
| | | | OFFSET[7:0] | | | | | | | |
| 3'b010 | GAIN | 0x01000000 | GAIN[23:16] | | | | | | | |
| | | | GAIN[23:16] | | | | | | | |
| | | | GAIN[15:8] | | | | | | | |
| | | | GAIN[7:0] | | | | | | | |
| 3'b011 | CONF | 0x00000000 | PSS | PDW | RS | RV | SHORT | A0_PSW | VRS | A1 |
| | | | A0 | 0 | 0 | 0 | FRS | FILTER | TPS | 0 |
| | | | 0 | DR[3] | DR[2] | DR[1] | DR[0] | FORMAT | BCS | DT |
| | | | CHKSUM | LATENCY | CLK1 | CLK0 | CS1] | CS[0] | 0 | 0 |

## OFFSET Register

**Table 6. OFFSET Register (Address = 3'b001)**

| BIT 31 | BIT 30 | BIT 29 | BIT 28 | BIT 27 | BIT26 | BIT 25 | BIT 24 |
|---|---|---|---|---|---|---|---|
| BIT 23 | BIT 22 | BIT 21 | BIT 20 | BIT 19 | BIT18 | BIT 17 | BIT 16 |
| BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT10 | BIT 9 | BIT 8 |
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| OFFSET[31] | OFFSET[30] | OFFSET[29] | OFFSET[28] | OFFSET[27] | OFFSET[26] | OFFSET[25] | OFFSET[24] |
| OFFSET[23] | OFFSET[22] | OFFSET[21] | OFFSET[20] | OFFSET[19] | OFFSET[18] | OFFSET[17] | OFFSET[16] |
| OFFSET[15] | OFFSET[14] | OFFSET[13] | OFFSET[12] | OFFSET[11] | OFFSET[10] | OFFSET[9] | OFFSET[8] |
| OFFSET[7] | OFFSET[6] | OFFSET[5] | OFFSET[4] | OFFSET[3] | OFFSET[2] | OFFSET[1] | OFFSET[0] |

Power-On/Reset value = 0x00000000

| Bits | Bit Name | Access | Reset | Description |
|---|---|---|---|---|
| 31:0 | OFFSET[31:0] | R/W | 0x00000000 | **Offset Calibration Bits:** The 32-bit word is signed number in 2's complement format. See Calibration section for more information. |

## GAIN Register

**Table 7. GAIN Register (Address = 3'b010)**

| BIT 31 | BIT 30 | BIT 29 | BIT 28 | BIT 27 | BIT26 | BIT 25 | BIT 24 |
|---|---|---|---|---|---|---|---|
| BIT 23 | BIT 22 | BIT 21 | BIT 20 | BIT 19 | BIT18 | BIT 17 | BIT 16 |
| BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT10 | BIT 9 | BIT 8 |
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| GAIN[31] | GAIN[30] | GAIN[29] | GAIN[28] | GAIN[27] | GAIN[26] | GAIN[25] | GAIN[24] |
| GAIN[23] | GAIN[22] | GAIN[21] | GAIN[20] | GAIN[19] | GAIN[18] | GAIN[17] | GAIN[16] |
| GAIN[15] | GAIN[14] | GAIN[13] | GAIN[12] | GAIN[11] | GAIN[10] | GAIN[9] | GAIN[8] |
| GAIN[7] | GAIN[6] | GAIN[5] | GAIN[4] | GAIN[3] | GAIN[2] | GAIN[1] | GAIN[0] |

Power-On/Reset value = 0x01000000

| Bits | Bit Name | Access | Reset | Description |
|---|---|---|---|---|
| 31:0 | GAIN[31:0] | R/W | 0x01000000 | **Gain Calibration Bits:** The 32-bit word is unsigned positive number in binary format. See Calibration section for more information. |

## Configuration Register (CONF)

**Table 8. CONF Register (Address = 3'b011)**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BIT 31 | BIT 30 | BIT 29 | BIT 28 | BIT 27 | BIT26 | BIT 25 | BIT 24 |
| BIT 23 | BIT 22 | BIT 21 | BIT 20 | BIT 19 | BIT18 | BIT 17 | BIT 16 |
| BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT10 | BIT 9 | BIT 8 |
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| PSS | PDW | RS | RV | SHORT | A0_PSW | VRS | A1 |
| A0 | 0 | 0 | 0 | FRS | FILTER | TPS | 0 |
| 0 | DR[3] | DR[2] | DR[1] | DR[0] | FORMAT | BCS | DT |
| CHKSUM | LATENCY | CLK1 | CLK0 | CS1] | CS[0] | 0 | 0 |

Power-On/Reset value = 0x00000000

| Bits | Bit Name | Access | Reset | Description |
|---|---|---|---|---|
| 31 | PSS | R/W | 1'b0 | **Power Save Select:**<br>0: Standby Mode (default)<br>1: Sleep Mode |
| 30 | PDW | R/W | 1'b0 | **Power Down Mode:**<br>0: Normal Mode (default)<br>1: Power Down Mode |
| 29 | RS | R/W | 1'b0 | **Reset System:**<br>0: Normal Operation (default)<br>1: Activate a Reset cycle. |
| 28 | RV | R | 1'bx | **Reset Indicator:** Read only. Bit is cleared to logic zero after the CONF register is read.<br>0: Normal Operation (default)<br>1: System was reset. |
| 27 | SHORT | R/W | 1'b0 | **Input Short:**<br>0: Normal Input (default)<br>1: Analog Inputs are disconnected from the pins and shorted internally to mid-supply ($V_{AVDD}$+$V_{AVSS}$)/2. |
| 26 | A0_PSW | R/W | 1'b0 | **Bridge Power-down Switch Function:** When this bit is set to 1, the output latch bit A0 is served as the switch control bit. The switch is closed to short pin A0 to DVSS with low on-resistor of typical 3 Ohms if the output latch bit is set to 1. The switch is open if the output latch bit is cleared. The switch remains active in standby mode and is forced to open in sleep mode.<br>0: Disabled (default)<br>1: Enabled. |
| 25 | VRS | R/W | 1'b0 | **Voltage Reference Select:** The input full-scale range is [-$V_{REF}$/(2xgain), $V_{REF}$/(2xgain)] with VRS=0, and is [-$V_{REF}$/gain, $V_{REF}$/gain] with VRS=1.<br>0: 2.5V<$V_{REF}$<($V_{AVDD}$-$V_{AVSS}$) (default)<br>1: 0.5V<$V_{REF}$<2.5V |
| 24 | A1 | R/W | 1'b0 | **Output Latch Bit:** This bit sets the value of the A1 output pin. During register read, this bit reflects the status of the A1 pin.<br>0: AVSS (default)<br>1: AVDD |

| | | | | |
|---|---|---|---|---|
| 23 | A0 | R/W | 1'b0 | **Output Latch Bit:** This bit sets the value of the A0 output pin. During register read, this bit reflects the status of the A0 pin.<br>0: AVSS (default)<br>1: AVDD |
| 22:20 | RESERVED | R/W | 3'b000 | **Reserved**<br>Always write 3'b000 |
| 19 | FRS | R/W | 1'b0 | **Filter Rate Select:**<br>0: Default output data rates. (default)<br>1: Scale the output data rate by a factor of 5/6. |
| 18 | FILTER | R/W | 1'b1 | **Digital Filter Configuration:** Configures the ADC digital filter<br>0: SINC5/SINC3 filter (default)<br>1: SINC5/SINC1 filter |
| 17 | TPS | R/W | 1'b0 | **Temperature Sensor Enable Bit:** The voltage output is about 125.4mV at room temp and the rate of change over temperature is about 420uV/°C. Amplifier gain is internally forced to 1 with buffer on for temperature sensor measurement.<br>0: Disabled (default)<br>1: Enabled. |
| 16:15 | RESERVED | R/W | 2'b00 | **Reserved**<br>Always write 2'b00 |
| 14:11 | DR[3:0] | R/W | 4'b0000 | **Data Rate Configuration:** Selects the ADC data rate.<br>0000: 120SPS (default)<br>0001: 60SPS<br>0010: 30SPS<br>0011: 15SPS<br>0100: 7.5SPS<br>1000: 3840SPS<br>1001: 1920SPS<br>1010: 960SPS<br>1011: 480SPS<br>1100: 240SPS<br>1101: 3.75SPS<br>1110: 1.875SPS |
| 10 | FORMAT | R/W | 1'b0 | **Data Format Bit:** This bit sets the ADC data format.<br>0: Bipolar mode (default)<br>1: Unipolar mode |
| 9 | BCS | R/W | 1'b0 | **Burnout Current Sources:** 1μA of current source is added to the input channel if enabled.<br>0: Disabled (default)<br>1: Enabled |
| 8 | DT | R/W | 1'b0 | **Delay Time Bit:** When set, the converter will wait for a delay time before starting a conversion. The delay time is 1280 SYSCLK cycles when FRS=0. And 1536 SYSCLK cycles when FRS=1.<br>0: No delay (default)<br>1: Delay time added |
| 7 | CHKSUM | R/W | 1'b0 | **ADC Data Checksum Enable Bit:**<br>0: Disabled (default)<br>1: Enabled |
| 6 | LATENCY | R/W | 1'b0 | **Zero Latency Bit:** When this bit is set, the ADC settles in one conversion cycle so that it functions as a zero latency ADC. |
| 5:4 | CLK[1:0] | R/W | 2'b00 | **Clock Select Bits:** These bits select the clock source for SYSCLK.<br>00: External crystal applied between OSC1 and OSC2. (default) |

| | | | | |
|---|---|---|---|---|
| | | | | 01: External clock applied to the OSC2 pin.<br>10: Internal 4.9152MHz clock with OSC2 tristated.<br>11: Internal 4.9152MHz clock with its output on OSC2 pin. |
| 3:2 | CS[1:0] | R/W | 2'b00 | **Channel Select Bits:**<br>00: Select physical channel 1: AIN1+/AIN1- (default)<br>01: Select physical channel 2: AIN2+/AIN2-<br>10: Reserved<br>11: Reserved |
| 1:0 | RESERVED | R/W | 2'b00 | **Reserved**<br>Always write 2'b00 |

## REVISION HISTORY

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| May 20, 2022 | | Initial release. |

## DISCLAIMER

Signal Micro reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

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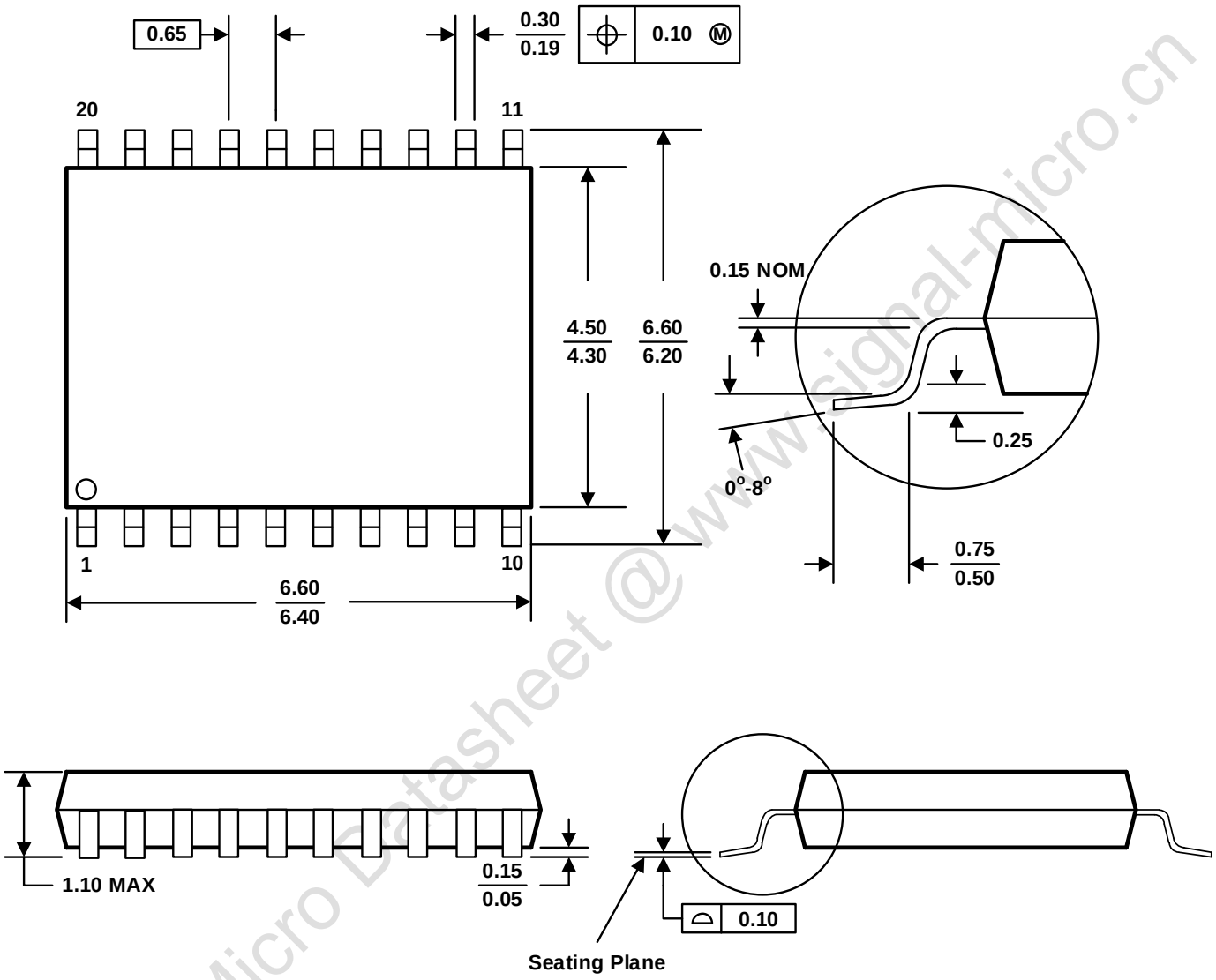
# PACKAGE OUTLINE DIMENSIONS

## TSSOP-20




**A. Compliant to JEDEC STARDARDS MO-153-AD.**
**B. All linear dimensions are in millimeters.**
**C. This drawing is subject to change without notice.**