JJMICROELECTRONICS

40V, 57A, 5.7mΩ N-channel Power SGT MOSFET

JMSH0406PK

Features

- Excellent $R_{DS(ON)}$ and Low Gate Charge
- 100% UIS Tested
- 100% ΔVds Tested
- Halogen-free; RoHS-compliant

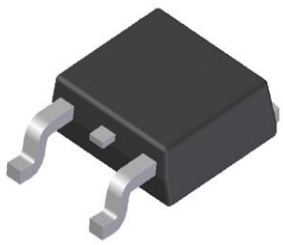
Applications

- Load Switch
- PWM Application
- Power Management

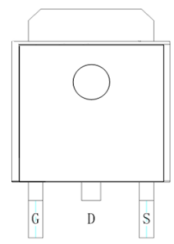
Product Summary

Parameters	Value	Unit
V_{DSS}	40	V
$V_{GS(th)\_Typ}$	1.7	V
I_D(@V_{GS}=10V)	57	A
$R_{DS(ON)\_Typ}$(@V_{GS}=10V	5.7	mΩ

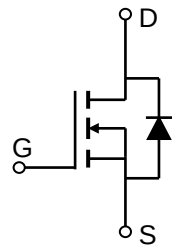
RoHS



TO-252-3L



Pin Assignment



Schematic Diagram

Ordering Information

Device	Marking	MSL	Form	Package	Reel(pcs)	Per Carton (pcs)
JMSH0406PK	SH0406P	3	Tape&Reel	TO-252-3L	2500	25000

Absolute Maximum Ratings (@ T_C = 25°C unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DS}	Drain-to-Source Voltage		40	V
V_{GS}	Gate-to-Source Voltage		±20	V
I_D	Continuous Drain Current	T_C = 25°C	57	A
		T_C = 100°C	36	
I_{DM}	Pulsed Drain Current (1)		Refer to Fig.4	A
E_{AS}	Single Pulsed Avalanche Energy (2)		89	mJ
P_D	Power Dissipation	T_C = 25°C	40	W
		T_C = 100°C	16	
T_J, T_{STG}	Junction & Storage Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient(3)	45	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.1	

Electrical Characteristics (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32V, V_{GS} = 0V	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1.2	1.7	2.2	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance(4)	V_{GS} = 10V, I_D = 20A	-	5.7	7.4	mΩ
Dynamic Characteristics						
R_g	Gate Resistance	f = 1MHz	-	0.9	-	Ω
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 20V, f = 1MHz	863	1208	1631	pF
C_{oss}	Output Capacitance		538	753	1016	pF
C_{rss}	Reverse Transfer Capacitance		51	71	96	pF
Q_g	Total Gate Charge	V_{GS} = 0 to 10V V_{DS} = 20V, I_D = 20A	15	20	28	nC
Q_{gs}	Gate Source Charge		-	6.3	-	nC
Q_{gd}	Gate Drain("Miller") Charge		-	6.1	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On DelayTime	V_{GS} = 10V, V_{DD} = 20V I_D= 20A, R_{GEN} = 3Ω	-	10	-	ns
t_r	Turn-On Rise Time		-	16	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	16	-	ns
t_f	Turn-Off Fall Time		-	5.8	-	ns
Body Diode Characteristics						
I_S	Maximum Continuous Body Diode Forward Current		-	-	57	A
I_{SM}	Maximum Pulsed Body Diode Forward Current		-	-	229	A
V_{SD}	Body Diode Forward Voltage	V_{GS} = 0V, I_S = 20A	-		1.2	V
trr	Body Diode Reverse Recovery Time	I_F = 20A, di/dt = 100A/us	23	32	43	ns
Qrr	Body Diode Reverse Recovery Charge		-	23	-	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
2. E_{AS} condition: Starting T_J=25C, V_{DD}=20V, V_{GS}=10V, R_G=25ohm, L=3mH, I_{AS}=7.7A, V_{DD}=0V during time in avalanche.
3. $R_{\theta JA}$ is measured with the device mounted on a 1inch^2 pad of 2oz copper FR4 PCB.
4. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%.

Typical Performance Characteristics

Figure 1: Power De-rating

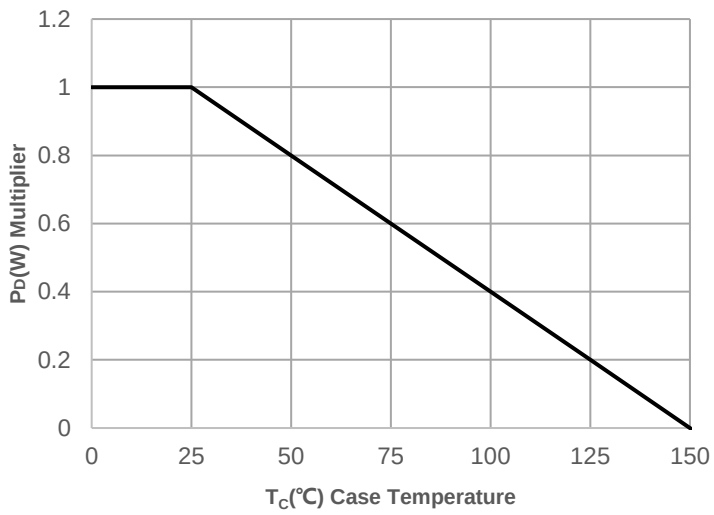


Figure 2: Current De-rating

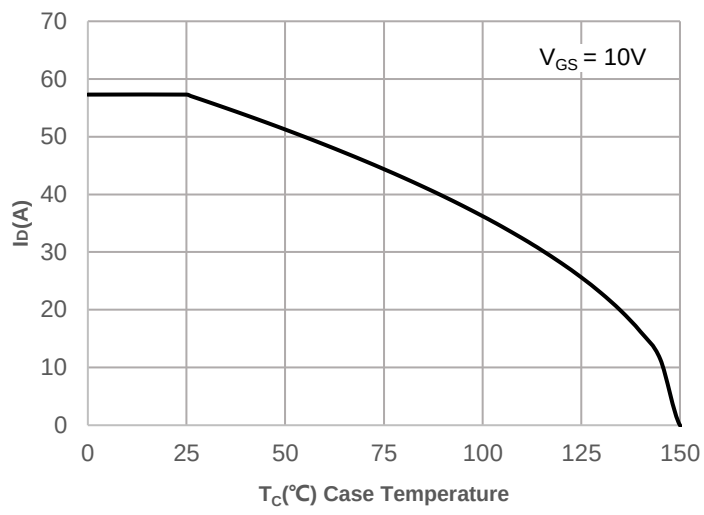


Figure 3: Normalized Maximum Transient Thermal Impedance

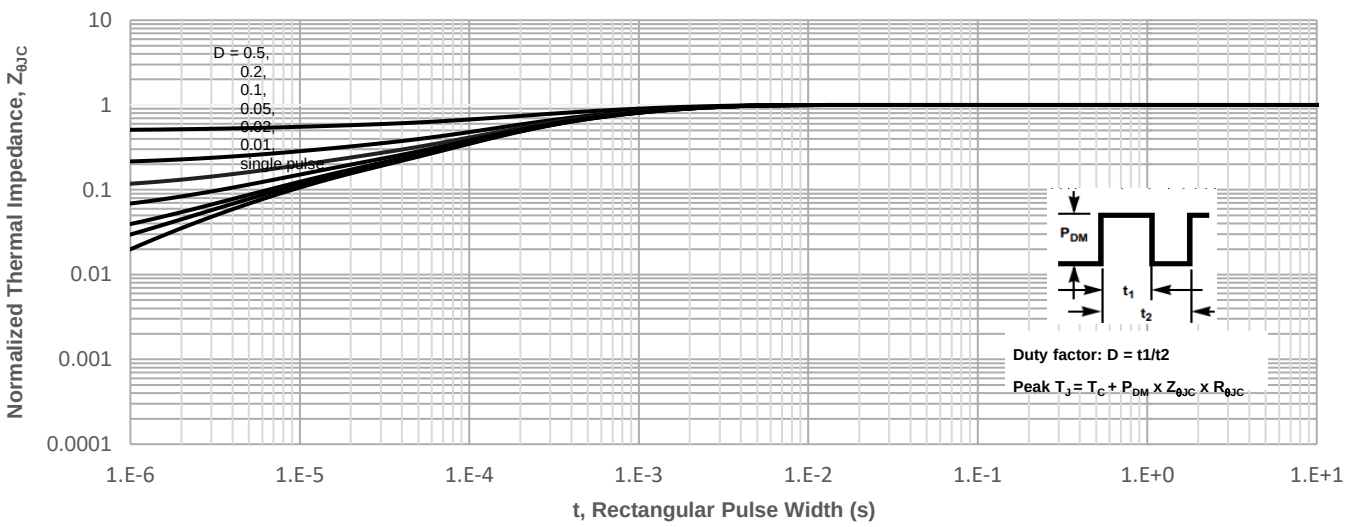
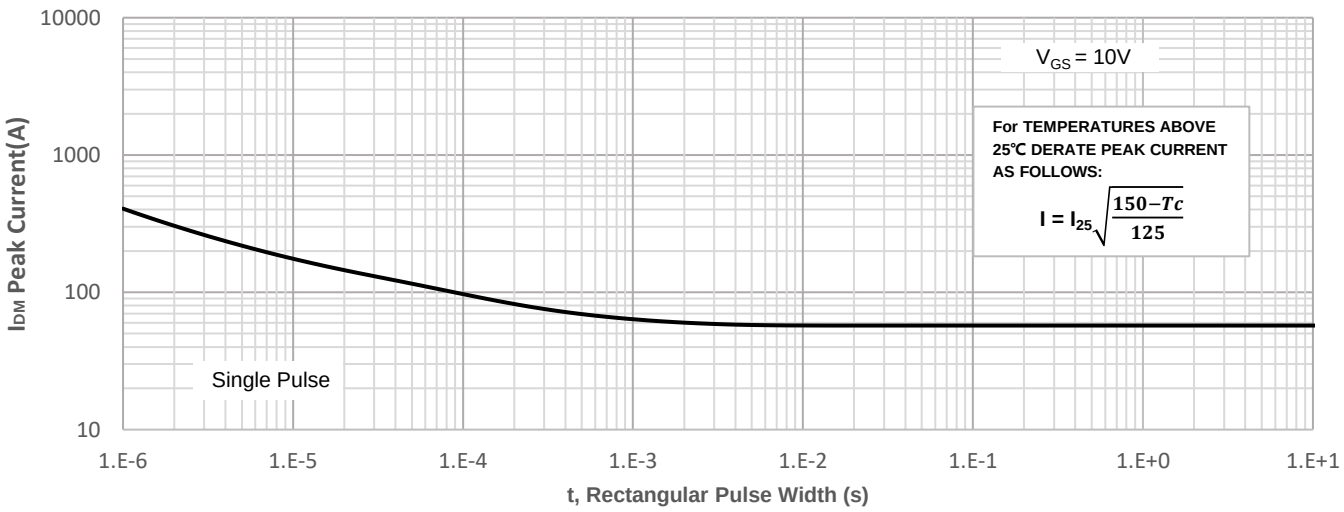


Figure 4: Peak Current Capacity



Typical Performance Characteristics

Figure 5: Output Characteristics

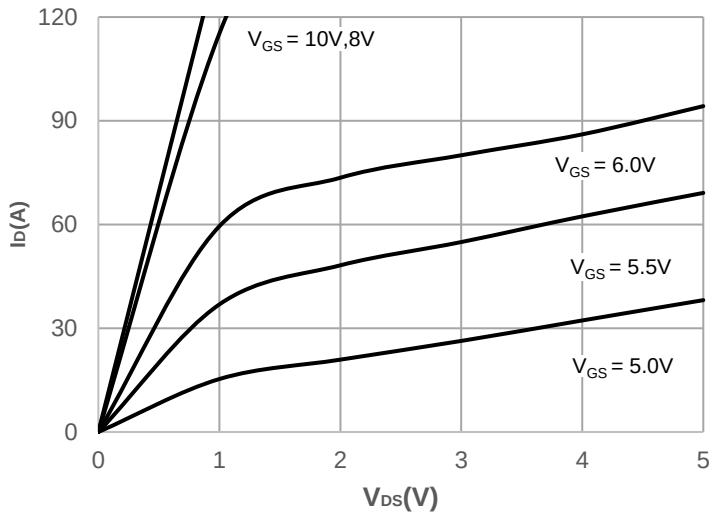


Figure 6: Typical Transfer Characteristics

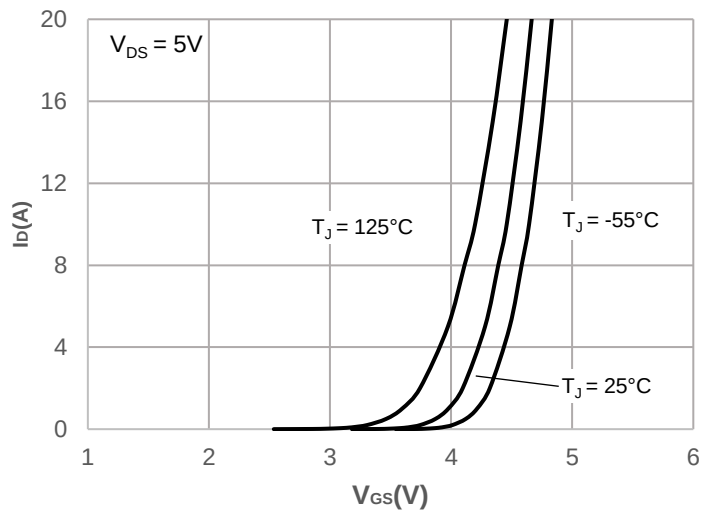


Figure 7: On-resistance vs. Drain Current

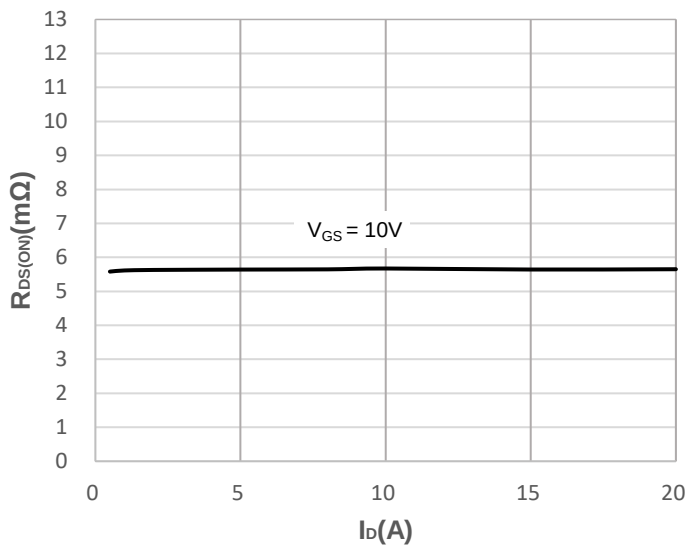


Figure 8: Body Diode Characteristics

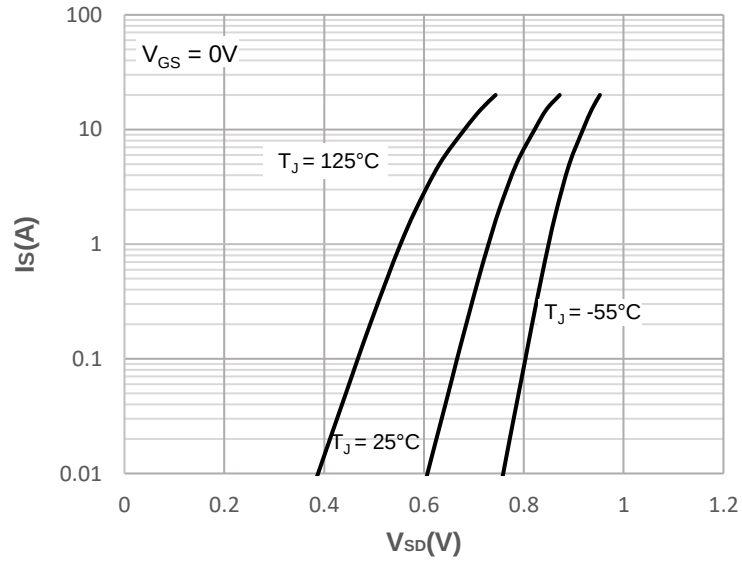


Figure 9: Gate Charge Characteristics

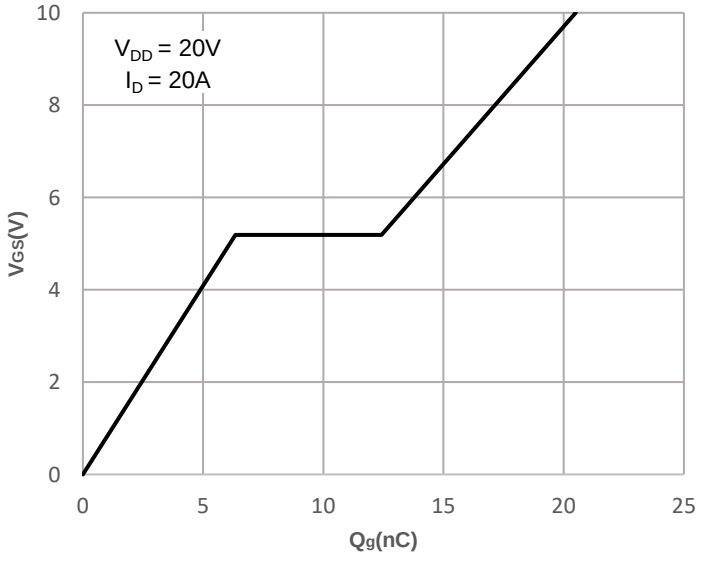
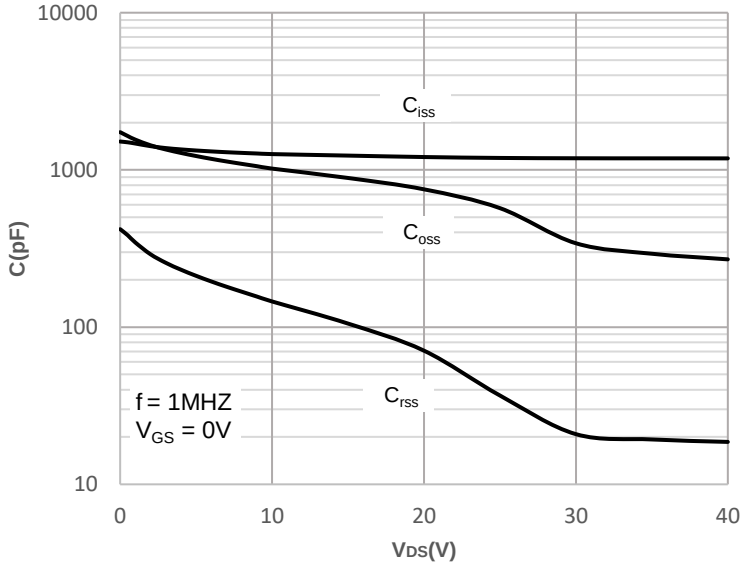


Figure 10: Capacitance Characteristics



Typical Performance Characteristics

Figure 11: Normalized Breakdown voltage vs. Junction Temperature

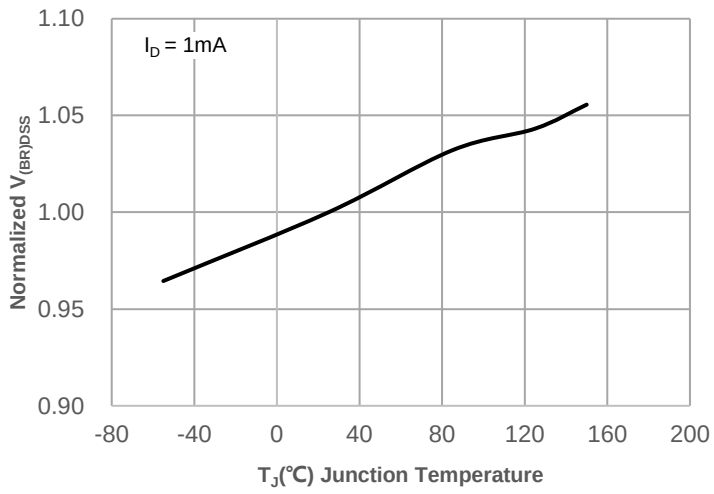


Figure 12: Normalized on Resistance vs. Junction Temperature

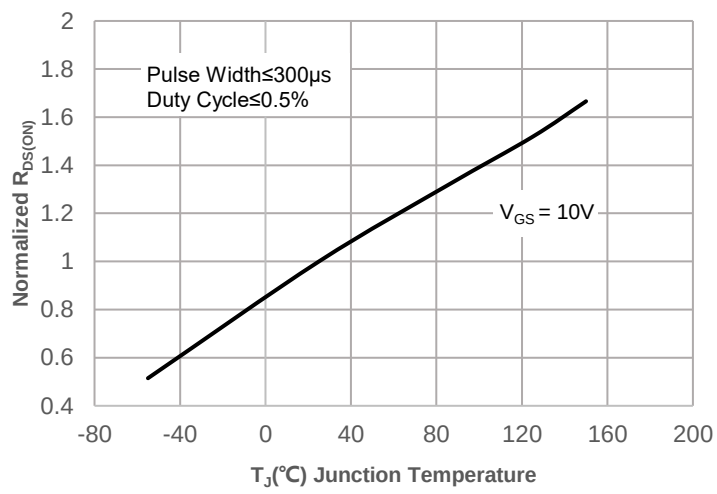


Figure 13: Normalized Threshold Voltage vs. Junction Temperature

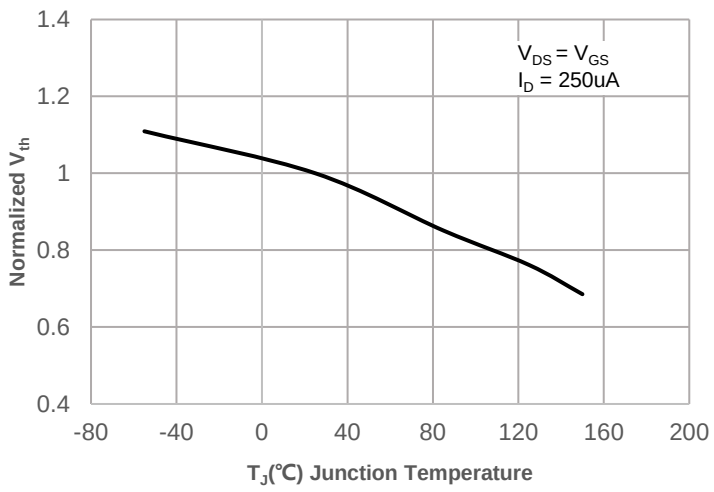


Figure 14: $R_{DS(ON)}$ vs. V_{GS}

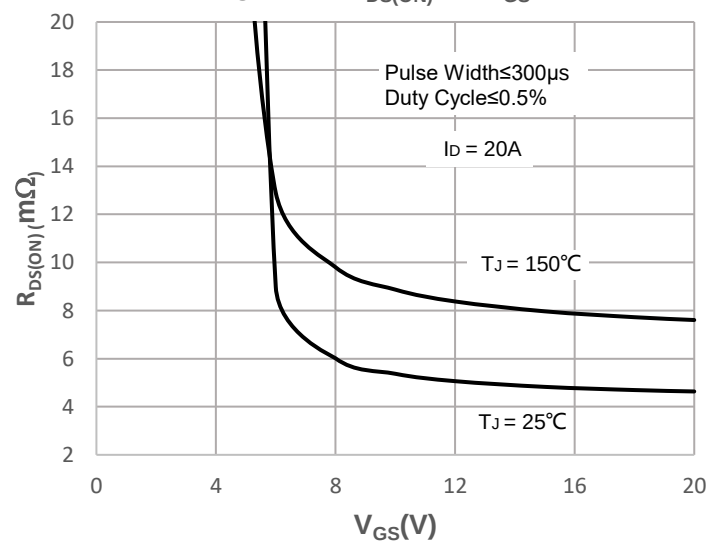
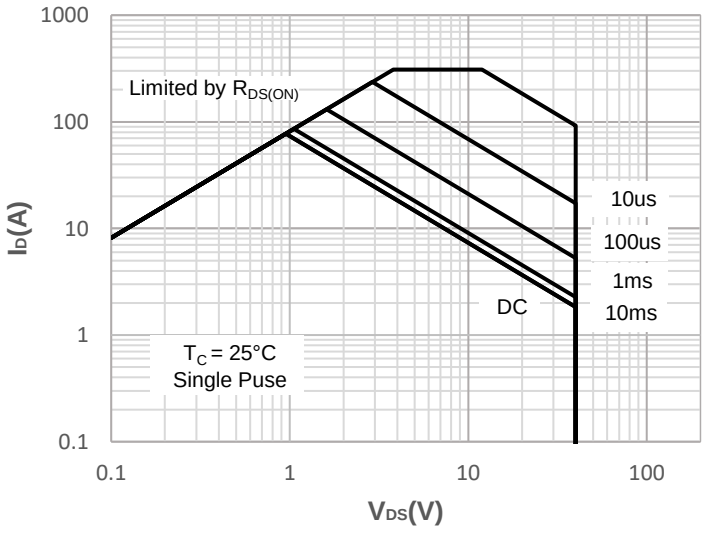


Figure 15: Maximum Safe Operating Area



Test Circuit

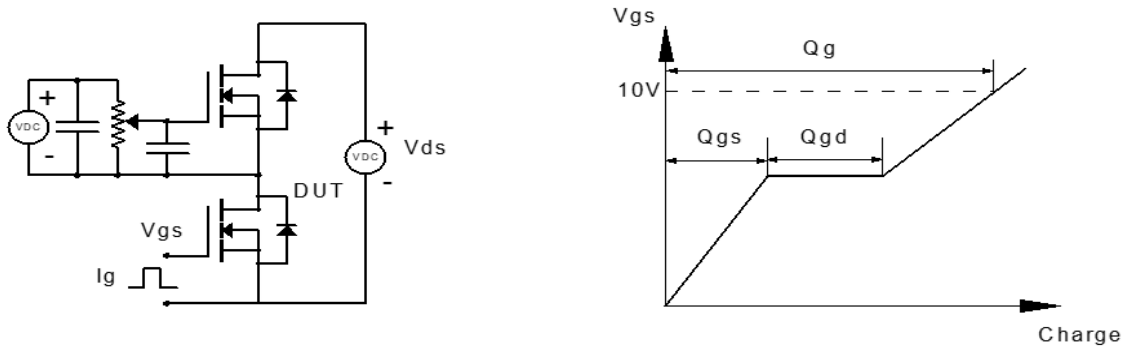


Figure 1: Gate Charge Test Circuit & Waveform

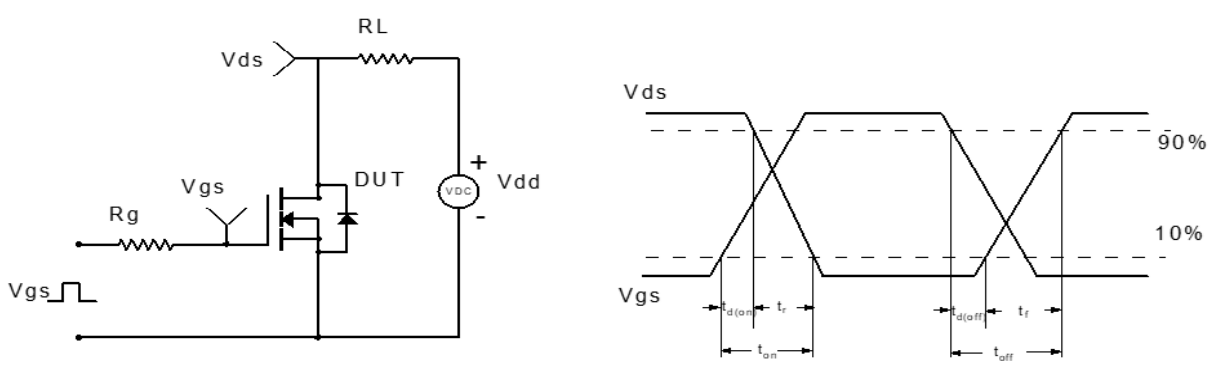


Figure 2: Resistive Switching Test Circuit & Waveform

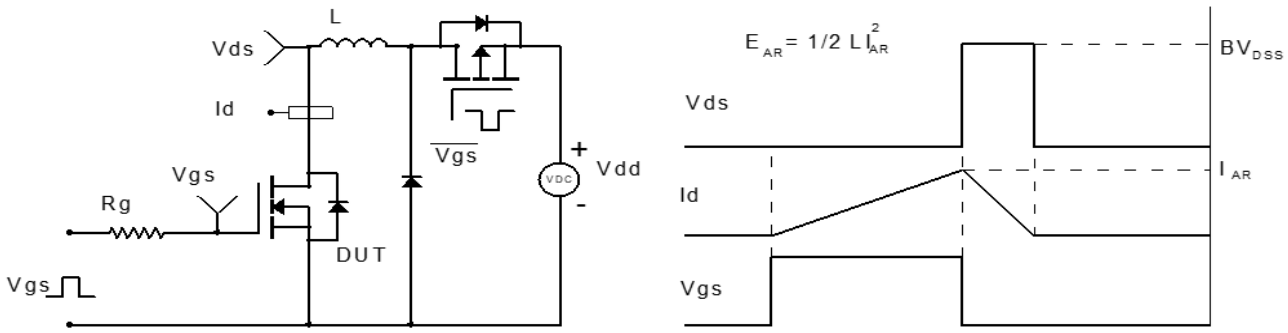


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

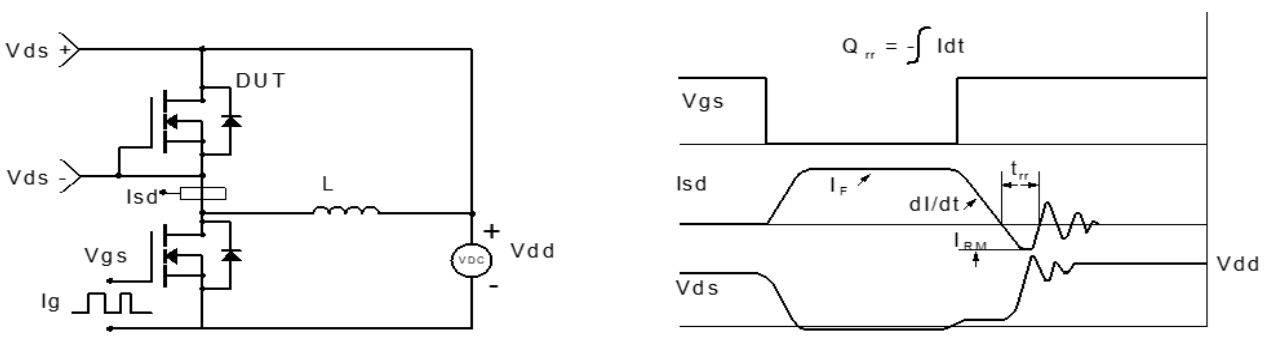
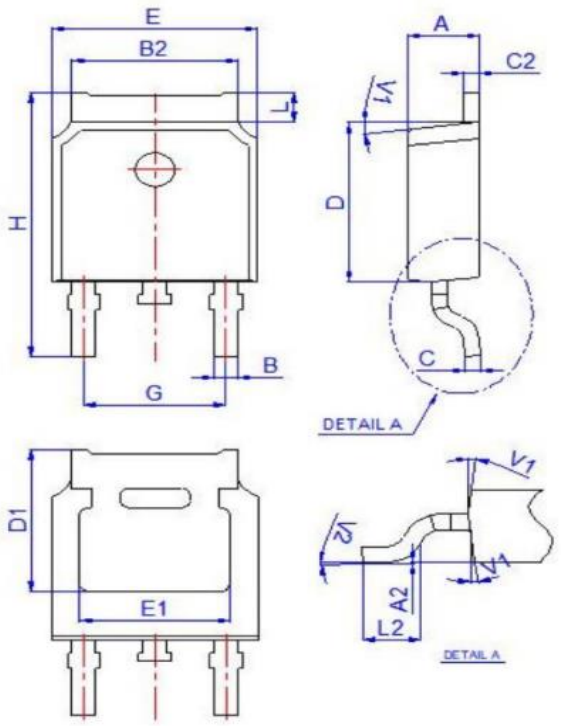


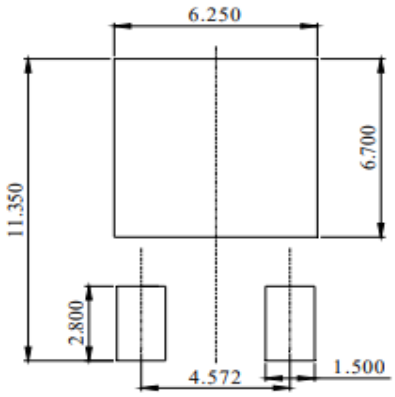
Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(TO-252-3L)



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Recommended Soldering Footprint



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