

# FR2307Z-VB Datasheet N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)		
100	0.0185 at V <sub>GS</sub> = 10 V	45	38 nC		

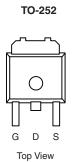
#### **FEATURES**

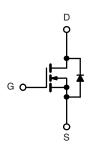
- TrenchFET® Power MOSFET
- 100 %  $\rm R_{\rm g}$  and UIS Tested





- Primary Side Switch
- Isolated DC/DC Converter





N-Channel MOSFET

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	100	V	
Gate-Source Voltage		V <sub>GS</sub> ± 20		v	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 25 °C		45 <sup>a</sup>	A	
	T <sub>C</sub> = 100 °C		30		
	T <sub>A</sub> = 25 °C	I <sub>D</sub>	9.2 <sup>b</sup>		
	T <sub>A</sub> = 100 °C		6.8 <sup>b</sup>		
Pulsed Drain Current		I <sub>DM</sub>	140	^	
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	1	45 <sup>a</sup>		
Continuous Source-Diam blode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	2 <sup>b</sup>		
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	35		
Avalanche Energy	L = U.T IIII	E <sub>AS</sub>	101	mJ	
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		136.4	w	
	T <sub>C</sub> = 100 °C	В	68.2		
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3 <sup>b</sup>		
	T <sub>A</sub> = 100 °C		1.5 <sup>b</sup>		
Operating Junction and Storage Temperature Ra	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b</sup>	Steady State	R <sub>thJA</sub>	40	50	°C/W
Maximum Junction-to-Case	Sieauy State	R <sub>thJC</sub>	0.85	1.1	C/VV

#### Notes:

- a. Package limited.
- b. Surface mounted on 1" x 1" FR4 board.



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100			V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 050 A		110		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	l <sub>D</sub> = 250 μA		- 12.5		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2.5		5	V
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zone Oata Walkana Busin Our	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V			1	
Zero Gate Voltage Drain Current		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	μΑ
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A		0.0185		Ω
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		33		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>			2400		pF
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		230		
Reverse Transfer Capacitance	C <sub>rss</sub>			80		
Total Gate Charge	$Q_g$			38	70	nC
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 50 \text{ A}$		14		
Gate-Drain Charge	Q <sub>gd</sub>			12		
Gate Resistance	$R_g$	f = 1 MHz		1.6	2.5	Ω
Turn-On Delay Time t <sub>d(on)</sub>				12	20	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 50 V, $R_L$ = 1 $\Omega$ $I_D \cong$ 50 A, $V_{GEN}$ = 10 V, $R_g$ = 1 $\Omega$		10	20	ns
Turn-Off Delay Time	t <sub>d(off)</sub>			18	35	
Fall Time	t <sub>f</sub>			8	15	
Drain-Source Body Diode Characteris	stics					
Continuous Source-Drain Diode	I <sub>S</sub>	T <sub>C</sub> = 25 °C			35	A
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>	_			100	
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 15 A		0.85	1.5	V
Body Diode Reverse Recovery Time t <sub>rr</sub>				80	120	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	$I_F = 50 \text{ A, dI/dt} = 100 \text{ A/}\mu\text{s, T}_J = 25 ^{\circ}\text{C}$		160	240	nC
Reverse Recovery Fall Time	t <sub>a</sub>			57		ns
Reverse Recovery Rise Time	t <sub>b</sub>			23		

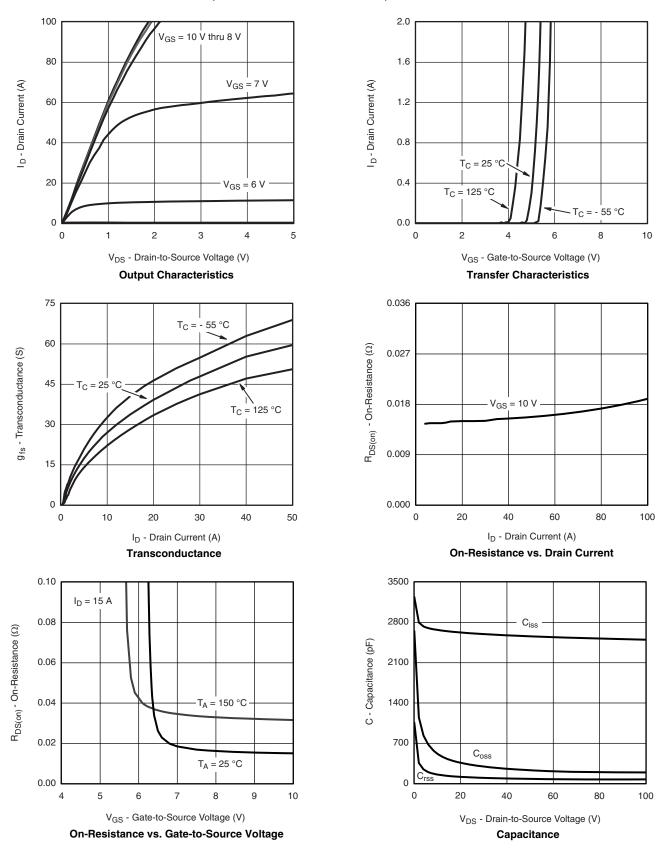
#### Notes:

- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise note)



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0

0.001

0.01

0.1

Time (s)

Single Pulse Power, Junction-to-Ambient

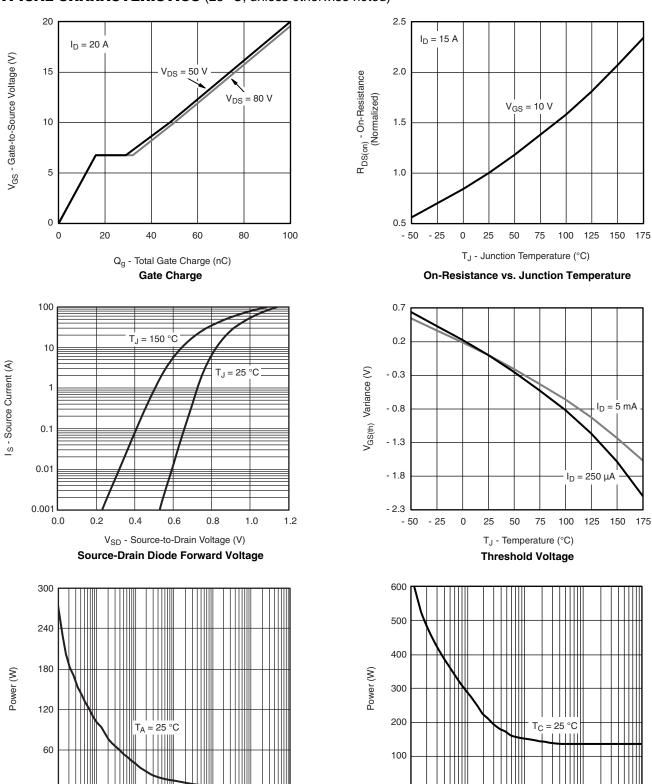
10

100

1000



### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



**4** 服务热线:400-655-8788

0.001

0.01

0.1

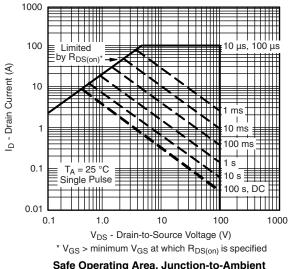
Time (s)

Single Pulse Power, Junction-to-Case

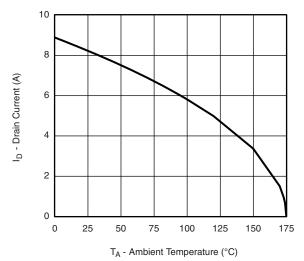
10



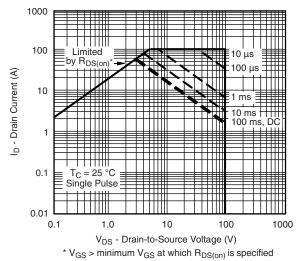
#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



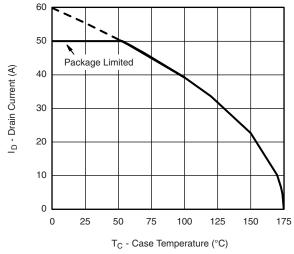




Current Derating\*\*, Junction-to-Ambient



Safe Operating Area, Junction-to-Case

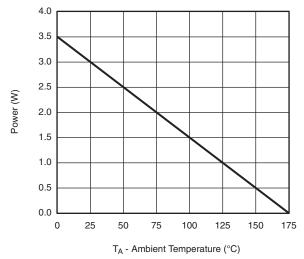


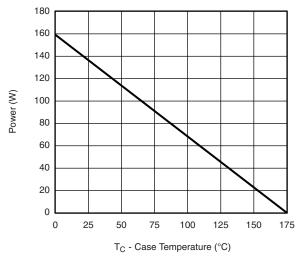
Current Derating\*\*, Junction-to-Case

<sup>\*\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max.)}$  = 175 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





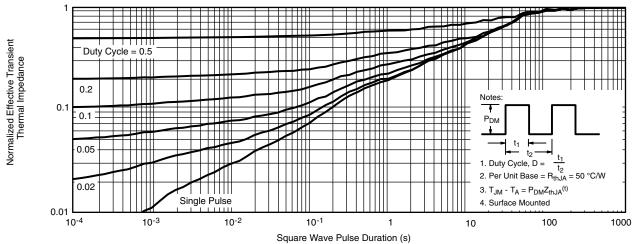
Power Derating\*\*, Junction-to-Ambient

Power Derating\*\*, Junction-to-Case

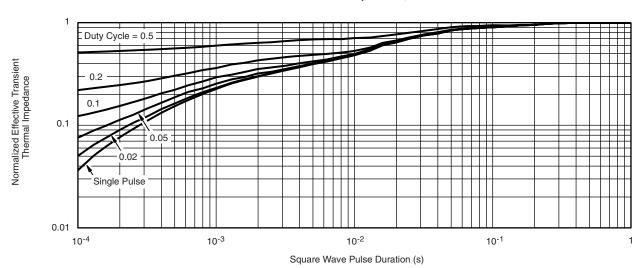
<sup>\*\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 175$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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