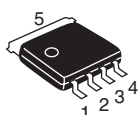


PSMN016-100YS-VB Datasheet

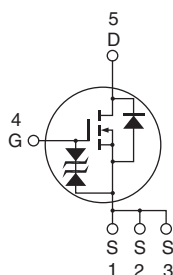
N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
100	0.0084 at V _{GS} = 10 V	75 ^a	17.1 nC
	0.0092 at V _{GS} = 6.0 V	65 ^a	
	0.0117 at V _{GS} = 4.5 V	54	



1, 2, 3 Source
4 Gate
5 Drain



FEATURES

- Trench Power MOSFET
- 100 % R_g and UIS Tested

APPLICATIONS

- Primary Side Switching
- Synchronous Rectification
- DC/AC Inverters
- LED Backlighting



RoHS
COMPLIANT
HALOGEN
FREE

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	A
		T _C = 70 °C	
		T _A = 25 °C	
		T _A = 70 °C	
Pulsed Drain Current (t = 100 μs)	I _{DM}	250	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	
Single Pulse Avalanche Current	I _{AS}	30	
Single Pulse Avalanche Energy	E _{AS}	45	mJ
Maximum Power Dissipation	P _D	T _C = 25 °C	W
		T _C = 70 °C	
		T _A = 25 °C	
		T _A = 70 °C	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	20	25	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	1.5	2.0	

Notes

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- The SOT-669 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 70 °C/W.

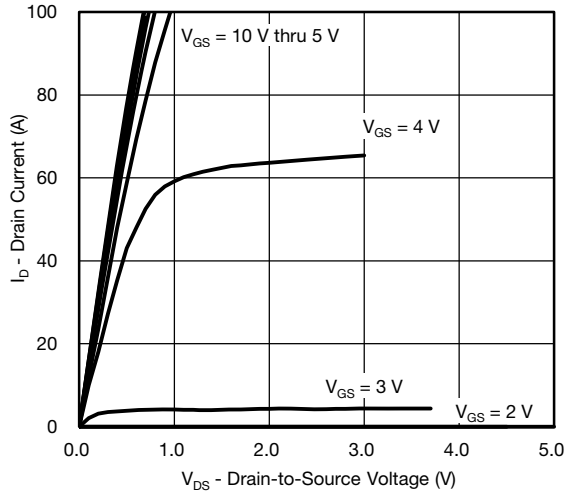
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	100			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		37		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 6.1		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.4		2.6	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V			1	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.0084		Ω
		V _{GS} = 6 V, I _D = 15 A		0.0092		
		V _{GS} = 4.5 V, I _D = 10 A		0.0117		
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 20 A		60		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz		1855		pF
Output Capacitance	C _{oss}			950		
Reverse Transfer Capacitance	C _{rss}			76		
Total Gate Charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 10 A		35.5	54	nC
		V _{DS} = 50 V, V _{GS} = 6 V, I _D = 10 A		22	33	
		V _{DS} = 50 V, V _{GS} = 4.5 V, I _D = 10 A		17.1	26	
Q _{gs}			5.3			
Q _{gd}			7.3			
Output Charge	Q _{oss}	V _{DS} = 50 V, V _{GS} = 0 V		57	86	
Gate Resistance	R _g	f = 1 MHz	0.5	1.3	2	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 4 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		12	24	ns
Rise Time	t _r			8	16	
Turn-Off DelayTime	t _{d(off)}			32	64	
Fall Time	t _f			7	14	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 40 V, R _L = 4 Ω I _D ≅ 10 A, V _{GEN} = 6.0 V, R _g = 1 Ω		14	28	
Rise Time	t _r			11	22	
Turn-Off DelayTime	t _{d(off)}			30	60	
Fall Time	t _f			8	16	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			75	A
Pulse Diode Forward Current (t = 100 μs)	I _{SM}				150	
Body Diode Voltage	V _{SD}	I _S = 5 A		0.76	1.1	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C		38	75	ns
Body Diode Reverse Recovery Charge	Q _{rr}			36	70	nC
Reverse Recovery Fall Time	t _a			19		ns
Reverse Recovery Rise Time	t _b			19		

Notes

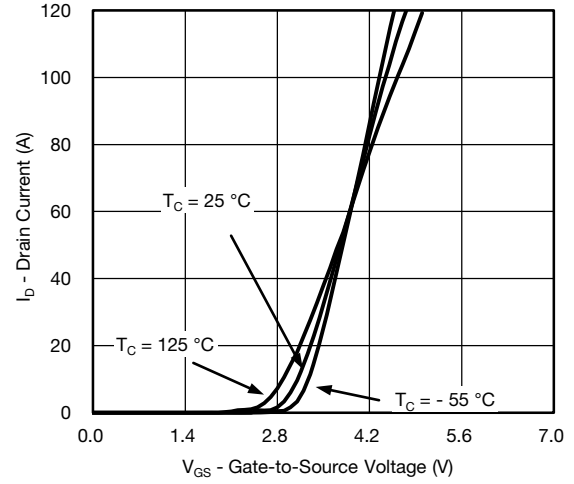
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

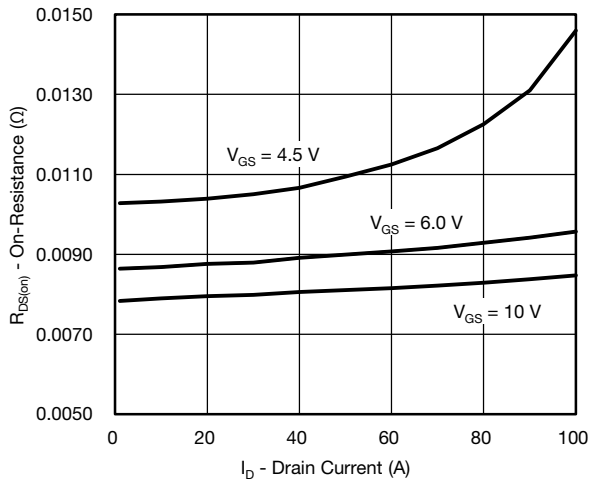
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



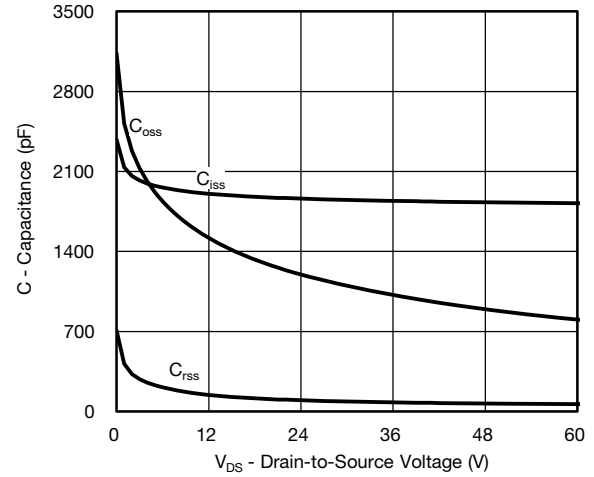
Output Characteristics



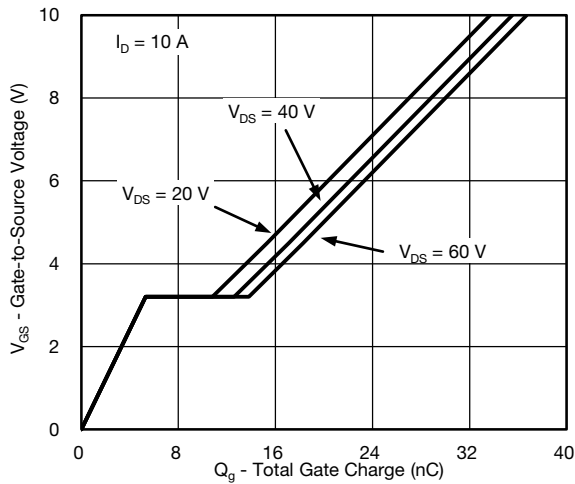
Transfer Characteristics



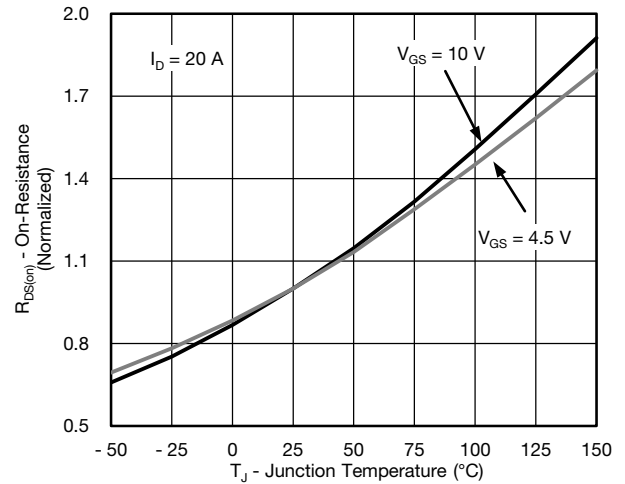
On-Resistance vs. Drain Current



Capacitance

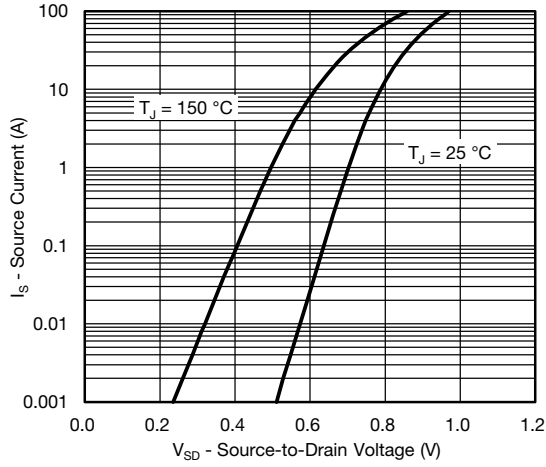


Gate Charge

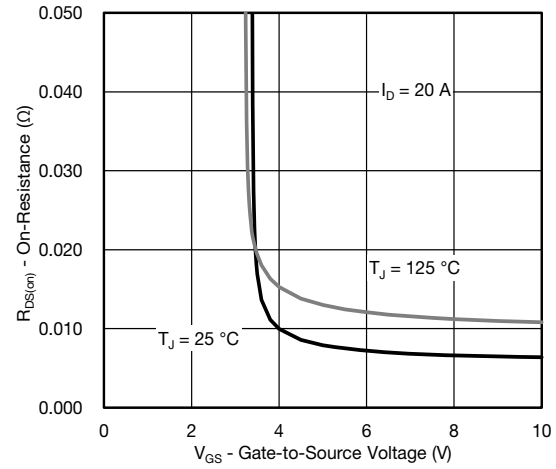


On-Resistance vs. Junction Temperature

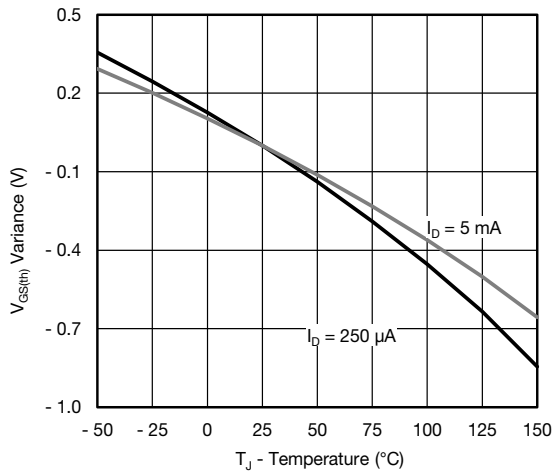
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



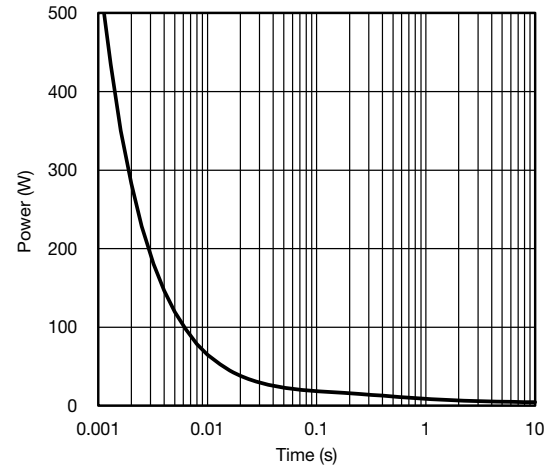
Source-Drain Diode Forward Voltage



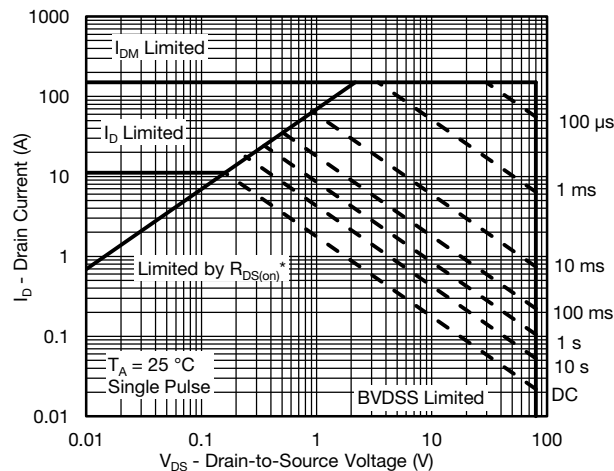
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



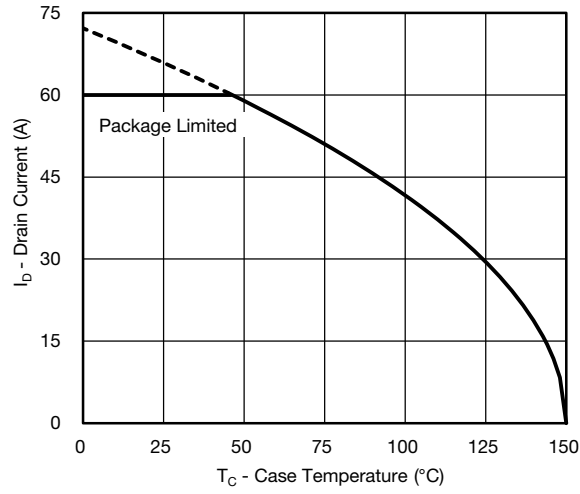
Single Pulse Power, Junction-to-Ambient



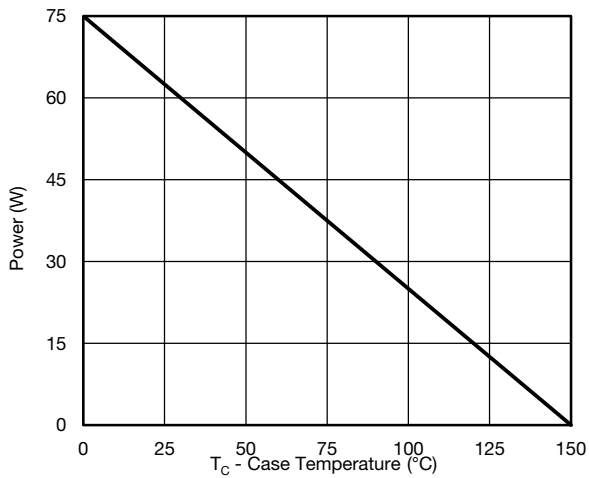
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

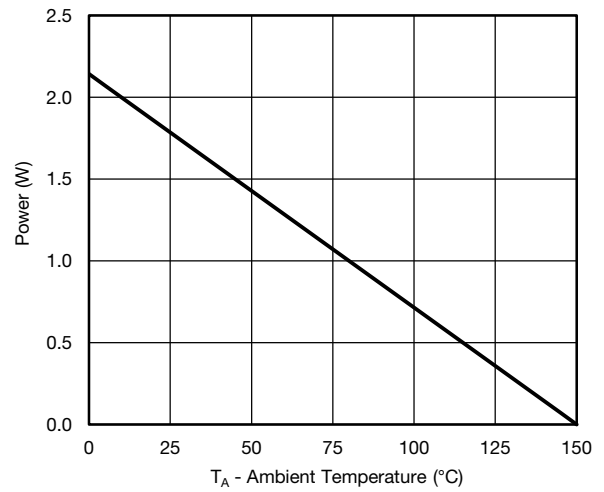
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



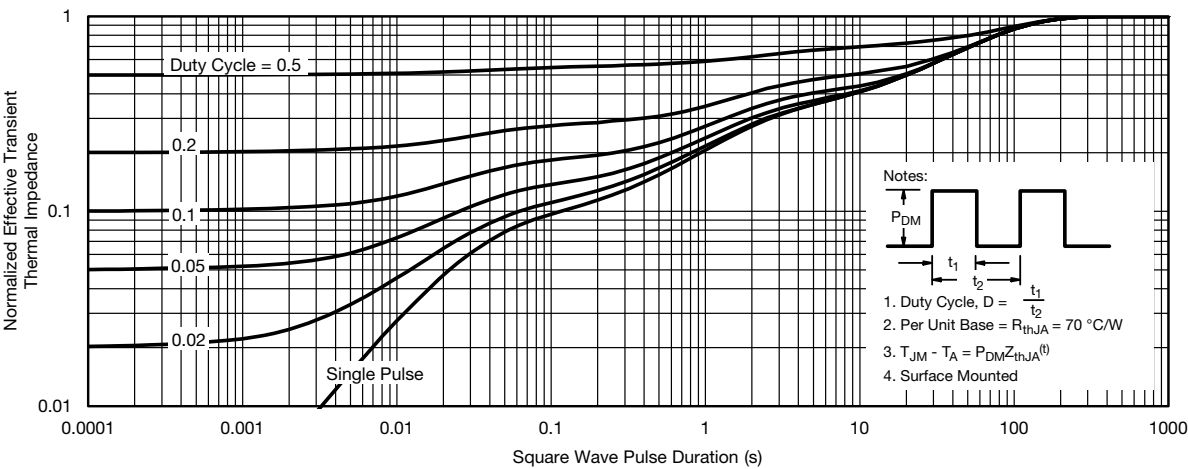
Power, Junction-to-Case



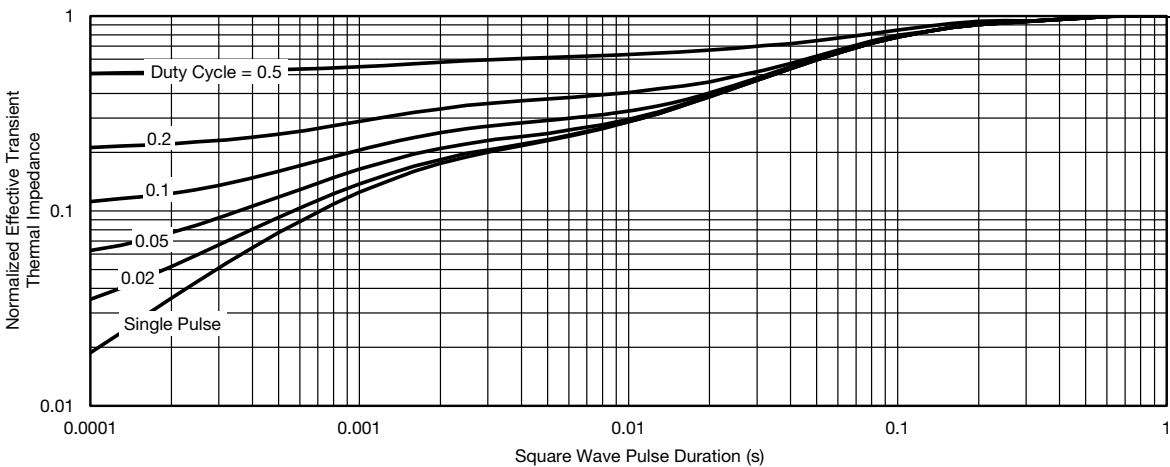
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

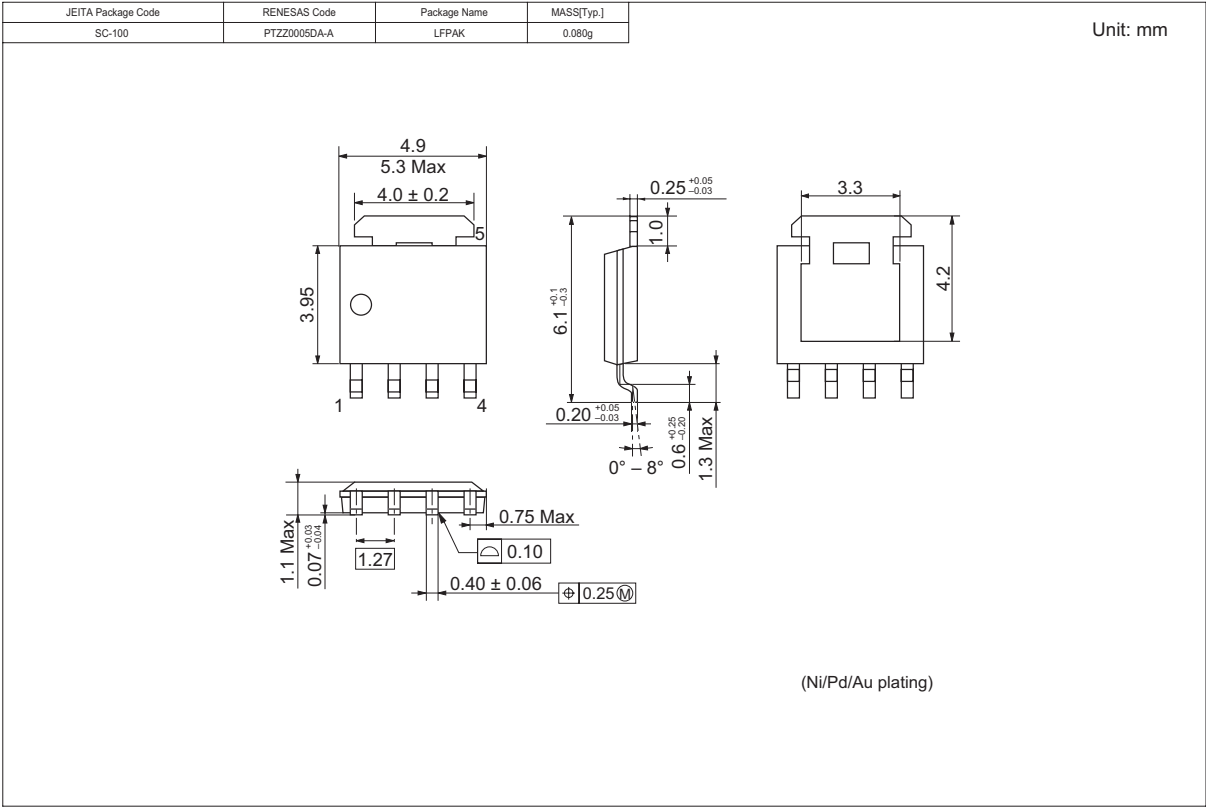


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Package Dimensions



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