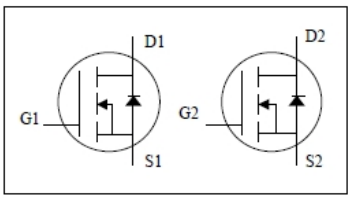
金易微半導體
Kingeavy Semiconductor

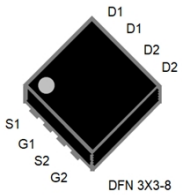
KE9202EAU

Dual N-CHANNEL
ENHANCEMENT MODE POWER

- **Simple Drive Requirement**
- **Fast Switching Characteristic**
- **Low On-resistence**
- **RoHS Compliant & Halogen-Free**



BV_{DSS}	30V
$R_{DS(ON)Typ}$	14mΩ
I_D	7A



Description

KE9202 is from Kingeavy innovated design and silicon process technology to achieve the lowest possible on- resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications

Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_A=25℃	Drain Current, V_{GS} @ 10V[3]	7	A
I_D@T_A=70℃	Drain Current, V_{GS} @ 10V[3]	5.2	A
I_{DM}	Pulsed Drain Current[1]	20	A
P_D@T_A=25℃	Total Power Dissipation	2.2	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	6	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	50	℃/W

Electrical Characteristics@T_j=25 oC(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
B_{VDSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=5A	-	14	16	mΩ
		V_{GS}=4.5V, I_D=3A	-	21.6	27	mΩ
VGS(th)	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	-	2.1	V
gfs	Forward Transconductance	V_{DS}=10V, I_D=5A	-	10	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V, V_{GS}=0V	-	-	10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Qg	Total Gate Charge	I_D=5A V_{DS}=15V V_{GS}=4.5V	-	6	9.6	nC
Qgs	Gate-Source Charge		-	2	-	nC
Qgd	Gate-Drain ("Miller") Charge		-	3	-	nC
td(on)	Turn-on Delay Time	V_{DS}=15V I_D=1A R_G=3.3Ω V_{GS}=10V	-	6	-	ns
tr	Rise Time		-	6	-	ns
td(off)	Turn-off Delay Time		-	15	-	ns
tf	Fall Time		-	3.5	-	ns
Ciss	Input Capacitance	V_{GS}=0V V_{DS}=15V f=1.0MHz	-	500	-	pF
Coss	Output Capacitance		-	85	-	pF
Crss	Reverse Transfer Capacitance		-	75	-	pF
Rg	Gate Resistance	f=1.0MHz	-	2	-	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage²	I_S=1A, V_{GS}=0V	-	-	1.2	V
t_{rr}	Reverse Recovery Time	I_S=5A, V_{GS}=0V dI/dt=100A/μs	-	14	-	ns
Q_{rr}	Reverse Recovery Charge		-	10	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board, t ≤10sec ; 90°C/W when mounted on min. copper pad.

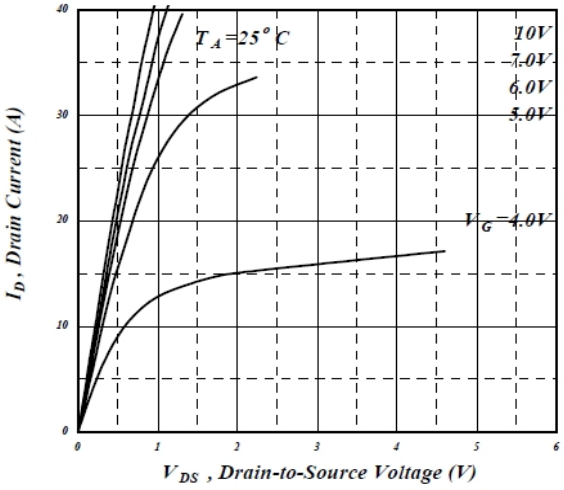


Fig 1. Typical Output Characteristics

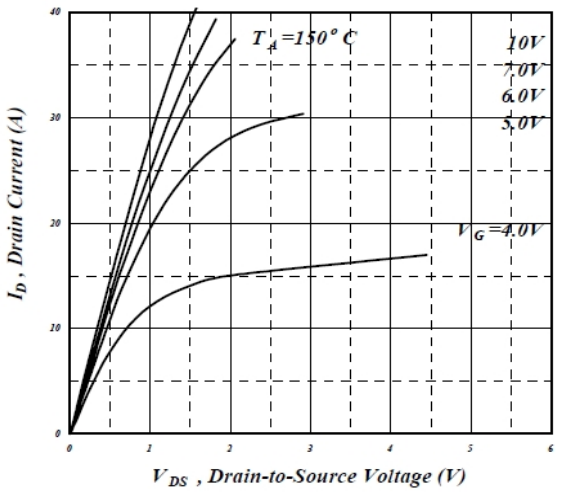


Fig 2. Typical Output Characteristics

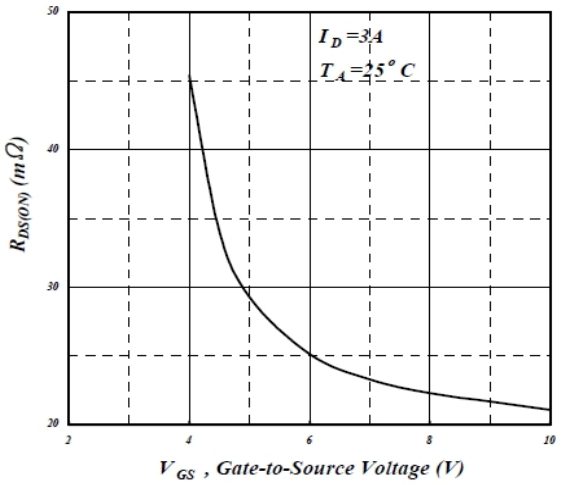


Fig 3. On-Resistance v.s. Gate Voltage

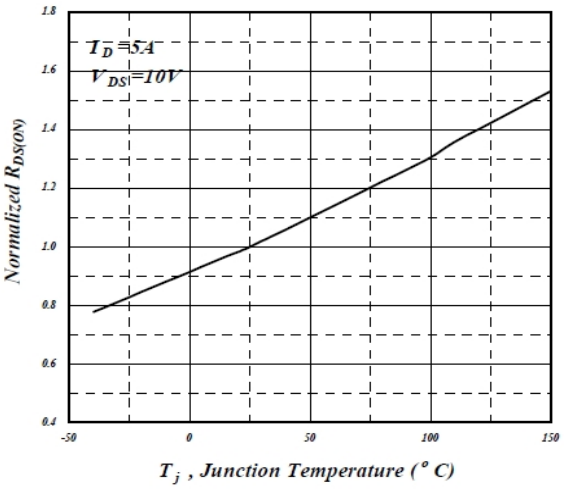


Fig 4. Normalized On-Resistance v.s. Junction Temperature

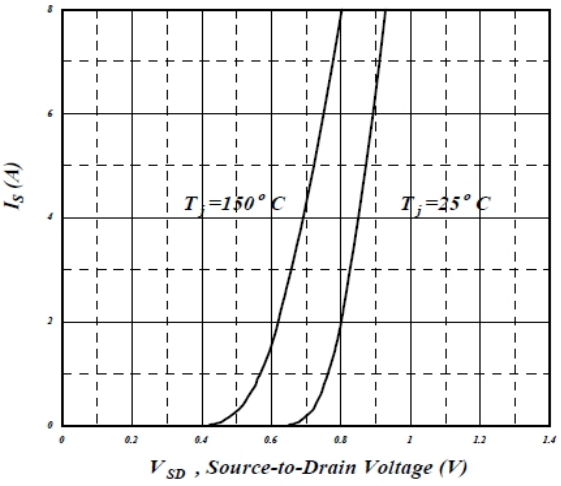


Fig 5. Forward Characteristic of Reverse Diode

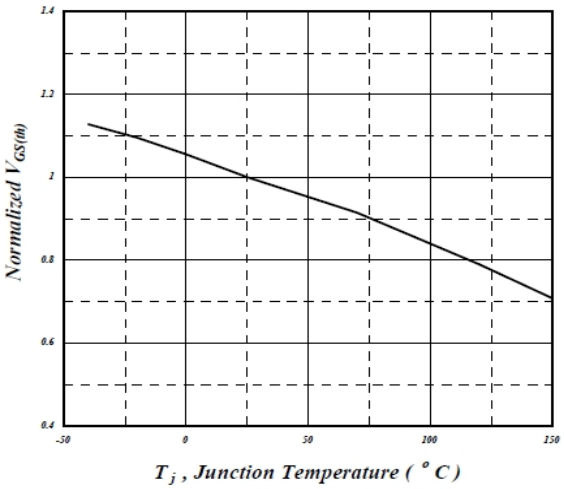


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

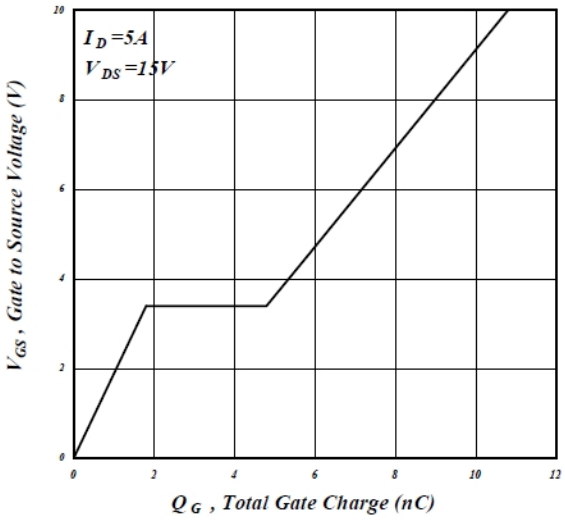


Fig 7. Gate Charge Characteristics

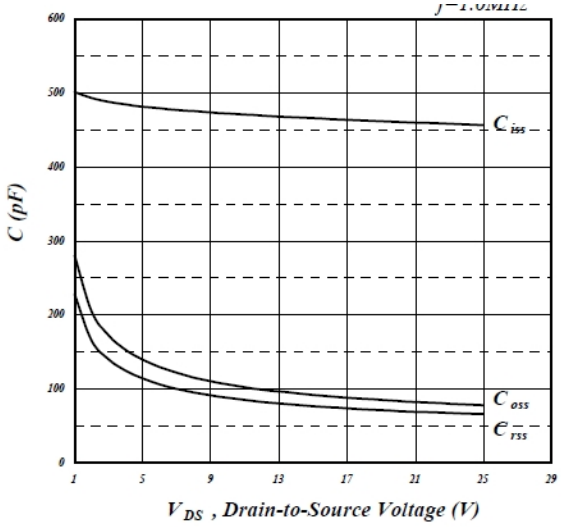


Fig 8. Typical Capacitance Characteristics

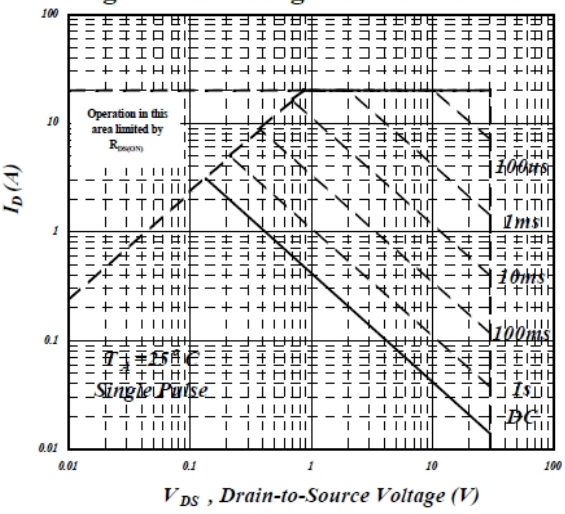


Fig 9. Maximum Safe Operating Area

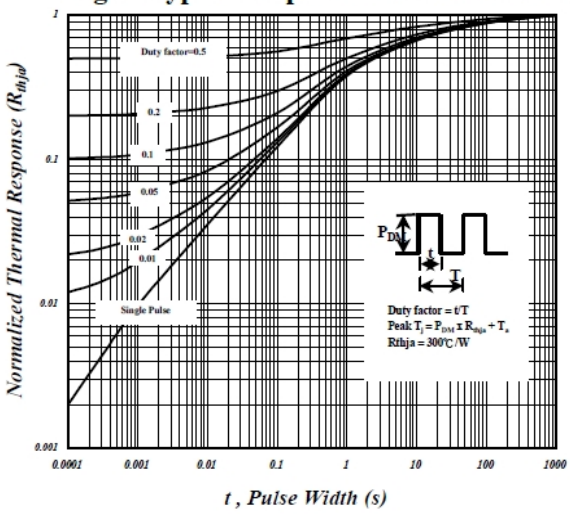


Fig 10. Effective Transient Thermal Impedance

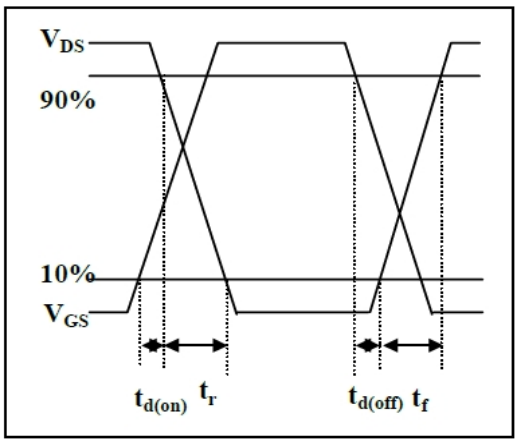


Fig 11. Switching Time Waveform

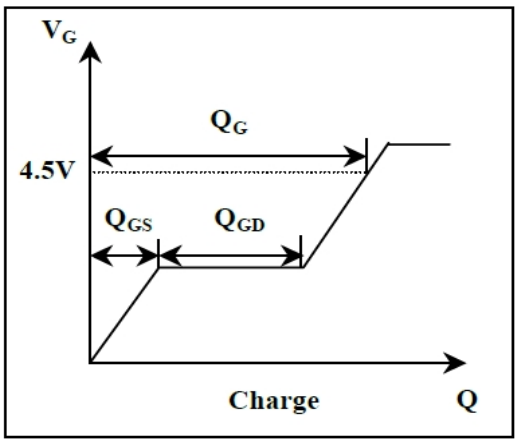
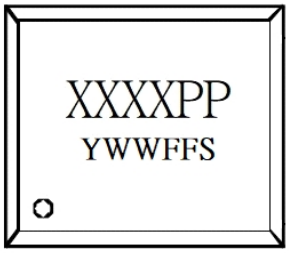


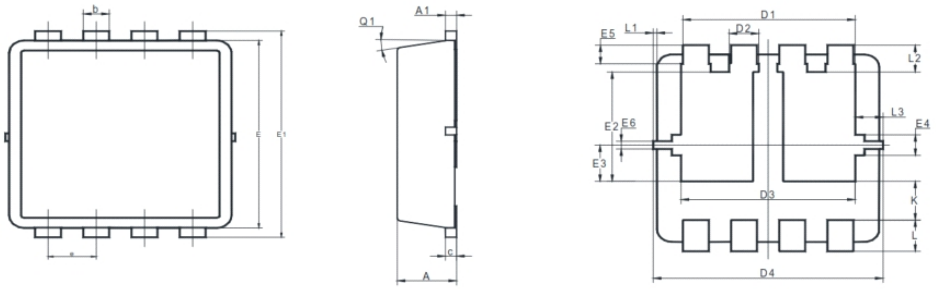
Fig 12. Gate Charge Waveform

Marking Information



Package	DFN3x3-8	
XXXX	Part Number	
PP	Package Code	
Y	Year	E=2019 , F=2020, ……
WW	Weeks	Ex. 10/27=44weeks, 11/3=45weeks
FF	Wafer lot	Lot No.
S	Serial	Serial No.
Dot	First pin	

Package Outline: DFN3x3-8



UNIT	A	A1	b	c	D	D1	D2	D3	D4	E	E1	E2	E3	E4
mm	0.9	0.05	0.35	0.25	3.1	2.45	0.5	2.7	3.2	3.1	3.3	1.85	0.68	0.43
	0.7	0	0.24	0.1	2.9	2.25	0.3	2.5	3	2.9	3.1	1.65	0.48	0.23

UNIT	E5	E6	e	K	L	L1	L2	L3	θ1
mm	0.4	0.175	0.7	0.72	0.5	0.1	0.53	0.475	12°
	0.2	0.075	0.6	0.52	0.3	0	0.33	0.275	0°

DFN 3x3 FOOTPRINT: