15W Power Over Ethernet PoE Powered Device (PD) Controller

Features

- Meets IEEE 802.3af Specifications
- 100V, 0.6Ω Integrated Pass Switch MOSFET
- 150mA inrush current limit
- 450mA DC Input Current Limit
- Over-temperature protection
- PGOOD with selectable logic and Inrush Completion Delay
- Intelligent Maintain Power Signature (MPS)
- SOP8 Package

Application

- VoIP Telephones
- Security Camera Systems
- Remote Internet Power
- Safety Backup Power
- Network Cards

Description

TMI7301 provides a complete interface for a powered device (PD) to comply with the IEEE® 802.3af standard in a Power-over-Ethernet (PoE) system. TMI7301 provides the PD with a detection signature, classification signature, and an integrated isolation power switch with inrush current control. During the inrush period, TMI7301 limit the current to less than 150mA before switching to the higher current limit (400mA to 500mA) when the isolation power MOSFET is fully enhanced. The device features an input UVLO with wide hysteresis and long deglitch time to compensate for twisted-pair cable resistive drop and to assure glitch-free transition during power-on/-off conditions. TMI7301 can withstand up to 100V at the input. TMI7301 also provides a power-good (PG) signal, two- step current limit and fold-back, over temperature protection, and di/dt limit. TMI7301 automatically generates the necessary pulsed current to maintain the PSE power. An external resistor is used to enable this functionality and to program the MPS pulsed current amplitude

Typical Application

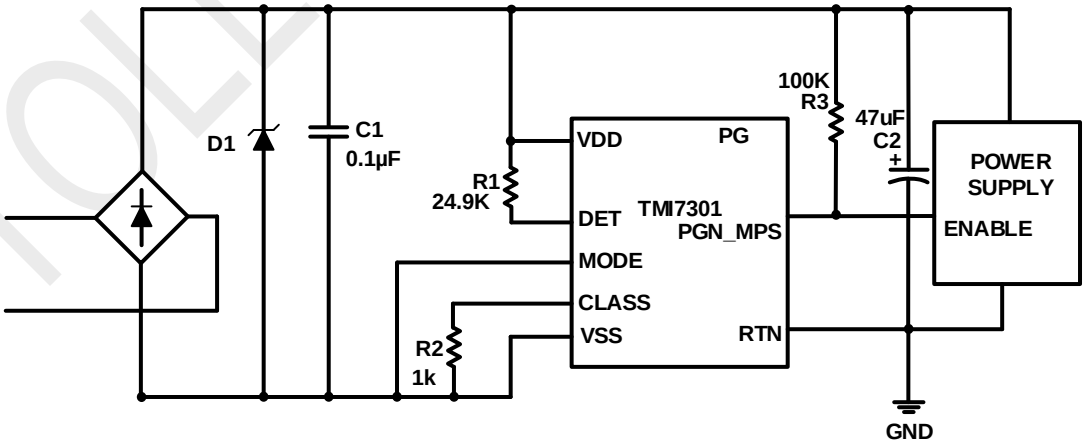


Figure 1. TMI7301 Typical Application Circuit

Absolute Maximum Ratings (Note 1)

Items	Min	Max	Unit
VDD, RTN, PGN_MPS，PG to VSS	-0.3	100	V
CLASS to VSS	-0.3	7	V
Junction Temperature	-40	150	°C
Lead Temperature		260	°C
Storage Temperature	-50	150	°C

Recommended Operating Conditions (Note 2)

Items	Min	Max	Unit
Supply Voltage VDD	0	57	V
Output Current IRTN	0	0.4	A
Operating Temperature	-40	85	°C
Operating Junction Temp	-40	125	°C

ESD Ratings

Items	Description	Value	Unit
$V_{(ESD-HBM)}$	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2017 Classification, Class: 2	±2000	V
$V_{(ESD-CDM)}$	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2018 Classification, Class: C3	±1000	V
$I_{LATCH-UP}$	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±200	mA

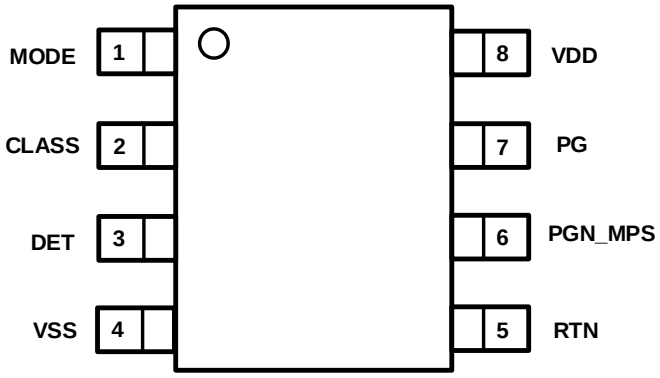
Thermal Resistance

Items	Description	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	116.3	°C/W
θ_{JC}	Junction-to-case(top) thermal resistance	53.7	°C/W
θ_{JB}	Junction-to-board thermal resistance	57.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.5	°C/W

Note 1: Exceeding these ratings may damage the device.

Note 2: The device is not guaranteed to function outside of its operating conditions.

Package



SOP8

Top Marking: T7301/XXXXX (T7301: Device Code, XXXXX: Inside Code)

Order Information

Part Number	Package	Top Marking	Quantity/ Reel
TMI7301	SOP8	T7301 XXXXX	3000

TMI7301 devices are Pb-free and RoHS compliant.

Pin Functions

Pin	Name	Function
1	MODE	Internally pulled up to internal 5V. Set The state of this pin determines the function of pin6&pin7.MODE is connected to VSS, PGN_MPS works as PGOOD indicator and PG works as MPS switch; MODE is floating, PG works as PGOOD indicator and PGN_MPS works as MPS switch.
2	CLASS	Classification Resistor Input. Connect a resistor (R_{CLS}) from CLS to VSS to set the desired classification current.
3	DET	Detection Resistor Input. Connect a signature resistor (R_{DET} = 24.9kΩ) from DET to VDD.
4	VSS	Negative Power Supply Terminal.
5	RTN	Isolate the drain of the MOSFET. RTN is connected to the ground of the subsequent DC-DC converter.
6	PGN_MPS	Open drain output. MODE=0, PGN_MPS work as PGOOD indicator, active-low output referenced to RTN.MODE=floating: PGN_MPS work as MPS switch.
7	PG	Open drain output. MODE=0, PG work as MPS switch MODE is floating: PG work as PGOOD indicator, active-high output referenced to RTN.
8	VDD	Positive power input. Connect a bypass capacitor of 68nF between VDD and VSS.

Electrical Characteristics

(V_{DD} = 48V, all voltages with respect to V_{SS}, V_{SS} = 0V; R_{DET} = 24.9kΩ, R_{CLASS} = 1000Ω, T_A = 25 ºC, unless otherwise noted.)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Detection							
Detection on	V_{DET_ON}	V_{VDD}=V_{RTN}=V_{PG}=1.9V			1.4		V
Detection off	V_{DET_OFF}	V_{VDD}=V_{RTN}=V_{PG}=12V		11	12	13	V
Detection on/off Hysteresis	V_{DET_H}	Falling below 12V on Threshold			1		V
DET Leakage Current	V_{DET_LK}	V_{DET}=V_{VDD}=57V, Measure I_{DET}			0.1	5	μA
Detection Current	I_{DET}	V_{VDD}=V_{RTN},R_{DET}=24.9kΩ, Measure I_{VDD}+I_{RTN}+I_{DET}	VDD=1.4V	55.1	56	56.9	μA
			VDD=10.1V	400	408	416	μA
Classification							
V_{CLASS} Output Voltage	V_{CL}	Over a Load Range of 1mA to 30mA			1.22		V
Classification Current	I_{CLASS0}	R_{CLASS}=1000Ω, 13≤V_{VDD}≤21V (guar by VCL)		1	1.2	2.8	mA
	I_{CLASS1}	R_{CLASS}=115Ω, 13≤V_{VDD}≤21V (guar by VCL)		10.3	10.6	11.3	
	I_{CLASS2}	R_{CLASS}=66.7Ω, 13≤V_{VDD}≤21V (guar by VCL)		17.7	18.3	19.5	
	I_{CLASS3}	R_{CLASS}=43Ω, 13≤V_{VDD}≤21V (guar by VCL)		27.1	28.4	29.5	
Classification Lower Threshold	V_{CL_ON}	Regulator Turns on, V_{VDD} Rising		11	12	13	V
Classification Upper Threshold	V_{CU_OFF}	Regulator Turns off, V_{VDD} Rising		21	22	23	V
	V_{CU_H}	Hysteresis			0.77		V
IC Supply Current during Classification	I_{IN_CLASS}	V_{DD} = 17.5V, CLASS Floating, RTN Tied to VSS		100	150	200	μA
Leakage Current	$I_{LEAKAGE}$	V_{CLASS} = 0 V, V_{VDD} = 57V				1	μA
Pass Device							
On Resistance	$R_{DS(ON)}$	I_{RTN}=300mA			0.6		Ω
Leakage Current	I_{SW_LK}	V_{VDD}=0,V_{RTN}=57V			1	15	μA
Current Limit	I_{LIMIT}	V_{RTN}=1V		400	450	500	mA
Inrush Limit	I_{INRUSH}	V_{RTN}=2V		120	150	200	mA
Fold-back threshold		V_{RTN} Rising		9.5	10	10.5	V
Fold-back deglitch time		V_{RTN} rising to when current limit changes to inrush current limit			345		μs
Inrush to Operating Mode Delay	t_{DELAY}	t_{DELAY} = minimum PG current pulse width after entering into power mode		80	94	110	ms
PGOOD-PG pin							
PG Sink Current		V_{RTN} = 1.5V, V_{PG} = 0.8V, during inrush period		130	230	330	μA
PG Off -leakage Current		V_{PG} = 48V			0.1	1	μA
PGOOD-PGN_MPS pin							
Output Low Voltage		Output Low Voltage I_{PG} =400μA			0.18	0.4	V
Leakage Current		V_{PG} =57 V, VRTN =0 V			0.1	1	μA

Electrical Characteristics

(V_{DD} = 48V, all voltages with respect to V_{SS}, V_{SS} = 0V; R_{DET} = 24.9kΩ, R_{CLASS} = 1000Ω, T_A = 25 ºC, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
MPS						
Automatic MPS falling current threshold	I_{MPS_TH}	Startup has completed, I_{RTN} falling threshold to generate MPS pulses		35		mA
Hysteresis on RTN current	HYS			3		mA
MPS pulsed mode duty cycle		MPS pulsed current ON time	65	75	85	ms
		MPS pulsed current OFF time	195	225	255	ms
		MPS pulsed current duty cycle	24.7%	25%	25.3%	
UVLO						
Voltage at VDD	V_{ON}	VDD Rising	37.2	38.6	40	V
	V_{OFF}	VDD Falling		31		
Thermal Shutdown						
Thermal Shut down Temperature (Note3)	T_{RISE}	Temperature Rising	140	152	160	ºC
Hysteresis	T_{HYS}			20		ºC
Bias Current						
Operating Current	$I_{Q(VDD)}$	VDD =48V, Pins 5,6 Floating Measure I_{VDD}		240	450	μA

Note 1: Guaranteed by design

Block Diagram

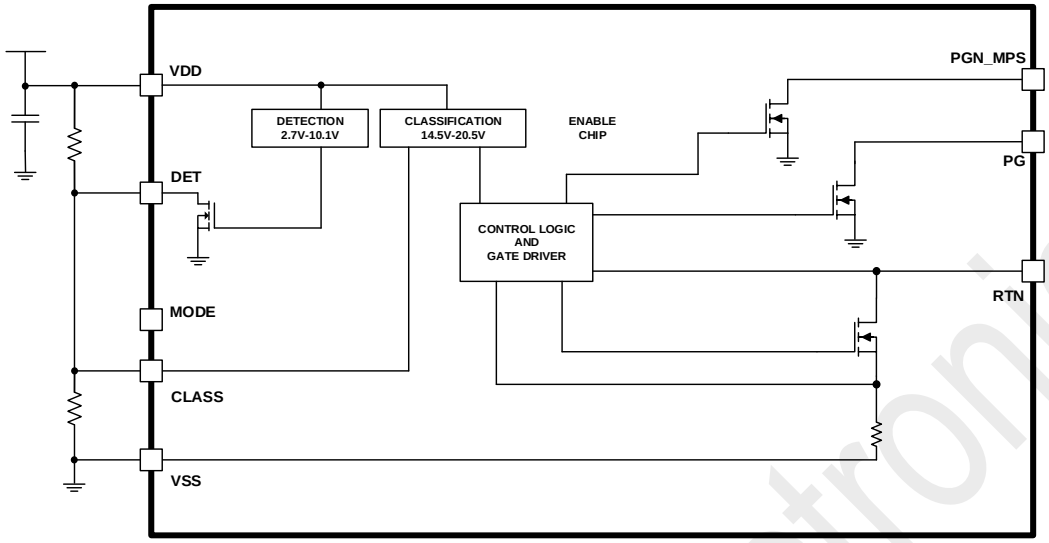


Figure 2 TMI7301 Block Diagram

Operation Description

Operating Mode

According to the different input voltage VDD, TMI7301 has 3 different working modes: PD detection, PD classification and PD power supply mode. When the input voltage is between 1.4V and 10.1V, the device enters PD detection mode; when the input voltage is between 12.6V and 20V, the device enters PD classification mode; once the input voltage exceeds V_{ON}, the device enters PD power supply mode.

Detection Mode (1.4V≤VDD≤10.1V)

In detection mode, PSE applies two voltages in the range of 1.4V to 10.1V (minimum step size is 1V) to VIN, and records the current measurement values at these two points. Then, PSE calculates DV/DI to ensure that the 24.9kΩ characteristic resistor is connected. Connect a characteristic resistor (R_{DET}) between VDD and DET to ensure correct feature detection. In detection mode, TMI7301 pulls DET low. When the input voltage exceeds 12.5V, DET becomes high impedance. In detection mode, most of the internal circuits of TMI7301 is in the off state, and the bias current is less than 10μA.

Classification Mode (12.6V≤VIN≤20V)

In the classification mode, the PSE classifies the PD according to the power consumption required by the PD, so that the PSE can effectively manage the power allocation. Connect an external resistor (R_{CLASS}) between CLASS and VSS to set the classification current. The PSE determines the PD level by applying a voltage to the PD input and measuring the current output by the PSE. When the voltage applied by the PSE is between 12.6V and 20V, the TMI7301 feeds back the classification current. PSE uses classification current information to classify PD power requirements. The classification current includes the current drawn by RCLS and the power supply current of TMI7301, so the total current drawn by PD is within the index range of IEEE802.3af standard. When the device is in power mode, the classification current is turned off.

Power Mode

When VIN rises above the undervoltage lockout threshold (V_{ON}), TMI7301 enters the power supply mode. When VIN rises above V_{ON}, TMI7301 turns on the internal n-channel isolation MOSFET, connects VSS to RTN, and the internal inrush current limit is set to 150mA. When the voltage at RTN approaches VSS and the inrush current falls below the inrush threshold, the isolation MOSFET is fully turned on. Once the isolation MOSFET is fully turned on, TMI7301 changes the current limit to 450mA. Before the power MOSFET is fully turned on, the power-good open-drain output remains turned off for a duration of at least t_{DELAY} to prohibit subsequent DC/DC converters during the surge.

Undervoltage Lockout

The working voltage of TMI7301 is as high as 57V, the UVLO threshold (V_{ON}) of the circuit is =38.6V; the UVLO threshold (V_{OFF}) of the circuit is 31V. When the input voltage is higher than V_{ON}, TMI7301 enters the power supply mode and the internal MOSFET turns on. When the input voltage is lower than V_{OFF} for more than t_{OFF_DLY}, the MOSFET turns off. The power-good output uses an open-drain output to disable subsequent DC-DC converters before the n-channel isolation MOSFET is fully turned on. Before the internal isolation MOSFET is fully turned on, the PG switch is off, and the hold time is t_{DELAY}. When exiting the thermal shutdown state, the PG switch is also off.

PGOOD Output of PGN_MPS

PGN_MPS is an active low output that is pulled to VSS when the device is in the steady-state power mode. It remains in a high impedance state at all other times.

PGOOD Output of PG

PG is an active high output that is pulled to VSS when the device is in inrush phase. It remains in a high impedance state at all other times.

Maintain Power Signature

The MPS is an electrical signature presented by the PD to assure the PSE that it is still present after operating voltage is applied. For IEEE802.3af/at PD, a valid MPS consists of a minimum dc current of 10mA, or a 10mA pulsed current for at least 75ms every 325ms, and an AC impedance lower than 26.3kΩ in parallel with 0.05μF. The TMI7301 has 2 pins can generate MPS pulses. It is selectable through the MODE input pin. If the current through the RTN-to-VSS path is below about 28mA, the TMI7301 automatically generates the MPS pulsed current through the PGN_MPS(PG) output pin, the current amplitude being adjustable with an external resistor.

Thermal Shutdown Protection

TMI7301 has thermal shutdown protection function to avoid overheating. If the junction temperature exceeds the 150°C thermal shutdown threshold, the TMI7301 will turn off the internal power MOSFET. When the junction temperature drops below 130°C, the device enters surge mode and then returns to power mode. Surge mode ensures that the internal power MOSFET turns off the subsequent DC-DC converter before turning on.

PC Board Layout Consideration

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines for reference. Careful PCB layout is critical to achieve high efficiency and low EMI. Follow these layout guidelines for optimum performance:

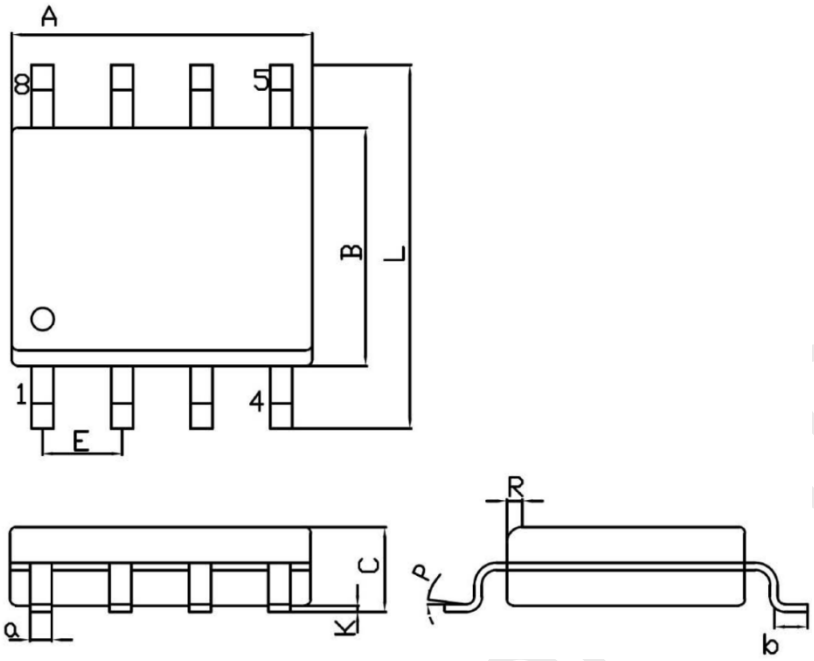
1) Place the input capacitor, classification resistor, and transient voltage suppressor as close as possible to the TMI7301.

2) Use large SMT component pads for power dissipating devices such as the TMI7301 and the external diodes.

3) Use short and wide traces for high-power paths

Package Information

SOP8



Unit: mm

Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min	Max		Min	Max
A	4.70	5.10	C	1.35	1.75
B	3.70	4.10	a	0.35	0.49
L	6.00	6.40	R	0.30	0.60
E	1.27 BSC		P	0°	7°
K	0.12	0.22	b	0.40	1.25

Note:

1) All dimensions are in millimeters.
2) Package length does not include mold flash, protrusion or gate burr.
3) Package width does not include inter lead flash or protrusion.
4) Lead popularity (bottom of leads after forming) shall be 0.10 millimeters max.
5) Pin 1 is lower left pin when reading top mark from left to right.

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