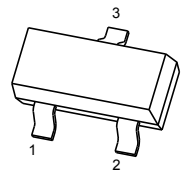
SOT-23 Plastic-Encapsulate MOSFETS

20V N-Channel Enhancement Mode MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	I_D Max
20V	28mΩ @ 4.5V	3.0A
	32mΩ @ 3.3V	

SOT-23

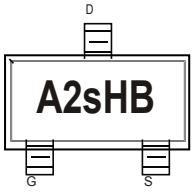


1. GATE
2. SOURCE 3
. DRAIN

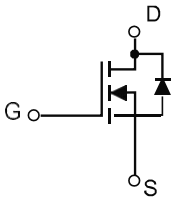
Features

Advanced trench process technology
High Density Cell Design For Ultra Low On-Resistance

MARKING



Equivalent circuit



PACKAGE SPECIFICATIONS

Package	Reel Size	Reel DIA. (mm)	Q'TY/Reel (pcs)	Box Size (mm)	Q'TY/Box (pcs)	Carton Size (mm)	Q'TY/Carton (pcs)
SOT-23	7'	178	3000	203×203×195	45000	438×438×220	180000

Maximum Ratings (TA = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±10	
Continuous Drain Current	T_A= 25 °C	I_D	3.0	A
	T_A = 70°C		2.5	
Pulsed Drain Current [1]		I_{DM}	12	A
Maximum Power Dissipation [1],[2]	T_A= 25 °C	P_D	1.2	W
	T_A = 70°C		0.9	
Maximum Junction Temperature		T_J	150	°C
Storage Temperature Range		T_{stg}	-50 to 150	°C
Thermal Resistance from Junction-to-Ambient (t≤5s)		$R_{\theta JA}$	100	°C/W

Notes
[1] Pulse width limited by maximum junction temperature.
[2] Surface Mounted on FR4 Board, t ≤ 5 sec.

The above data are for reference only.

MOSFET ELECTRICAL CHARACTERISTICS

T_a=25 ℃ unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Static						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D=250μA	20			V
Gate-body leakage	I_{GSS}	V_{GS}=±10V, V_{DS}=0V			±100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} =20V, V_{GS} =0V			1	μA
		V_{DS} =16V, V_{GS} =0V			100	μA
Gate-threshold voltage (note 1)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	0.4	0.6	1.0	V
Drain-source on-resistance (note 1)	$R_{DS(on)}$	V_{GS} =4.5V, I_D =3A		28	35	mΩ
		V_{GS} =3.3V, I_D =2A		32	40	
Forward transconductance (note 1)	g_{FS}	V_{DS} =5V, I_D =3.6A		8		S
Dynamic characteristics (note 2)						
Total Gate C harge	Q_g	V_{DS} =10V,I_D=3A,V_{GS} =5V		4.7		nC
Gate-Source Charge	Q_{gs}			0.6		
Gate-Drain Charge	Q_{gd}			1.7		
Input capacitance	C_{iss}	V_{DS} =10V,V_{GS} =0V, f=1MHz		280		pF
Output capacitance	C_{oss}			46		
Reverse transfer capacitance	C_{rss}			42		
Switching characteristics						
Turn-on delay time (note 2)	$t_{d(on)}$	V_{DD}=10V, V_{GS}=4.5V, I_D =4A,R_G=3.3Ω		11		ns
Rise time (note 2)	t_r			35		
Turn-off delay time (note 2)	$t_{d(off)}$			25		
Fall time (note 2)	t_f			32		
Drain-source body diode characteristics						
Source drain current(Body Diode)	I_{SD}				1.8	A
Body diode forward voltage (note 1)	V_{SD}	I_{SD}=2A, V_{GS} = 0V		0.74	1.2	V

Notes :

1. Pulse Test : Pulse Width≤ 300μs, Duty Cycle≤ 2 %.2
. These parameters have no way to verify.

Typical Characteristics

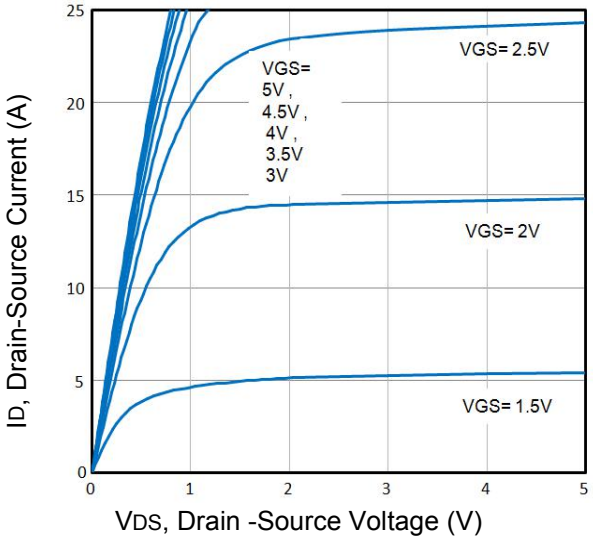


Fig1. Typical Output Characteristics

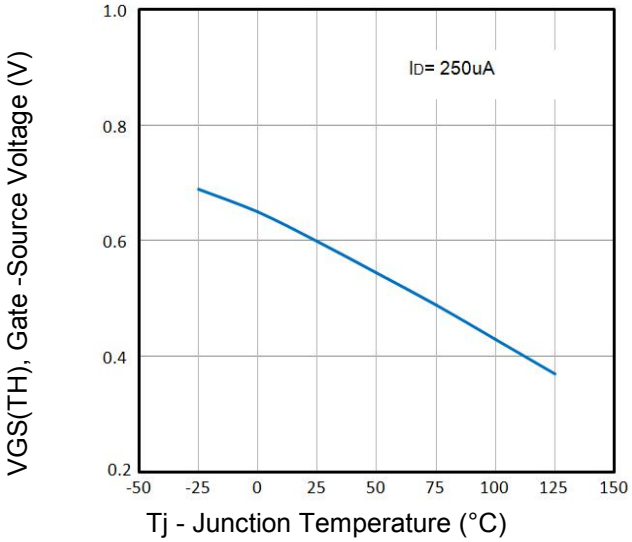


Fig2. Normalized Threshold Voltage Vs. Temperature

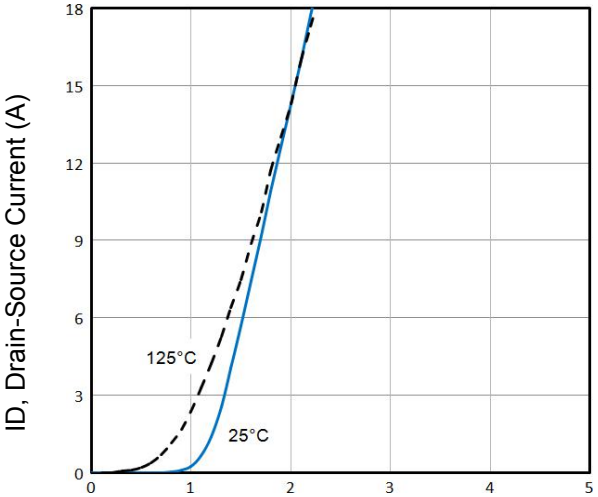


Fig3. Typical Transfer Characteristics

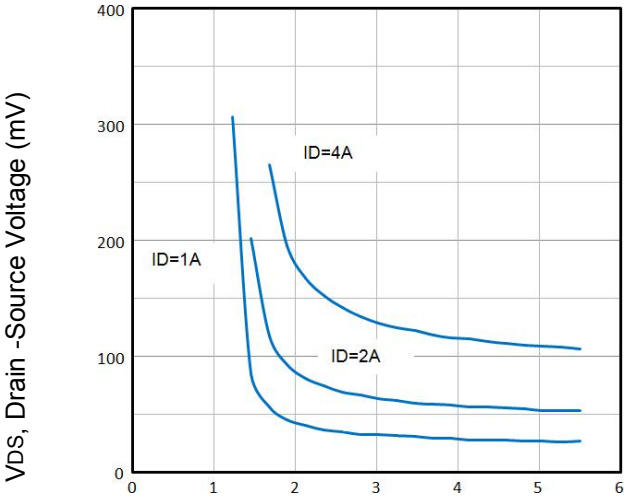
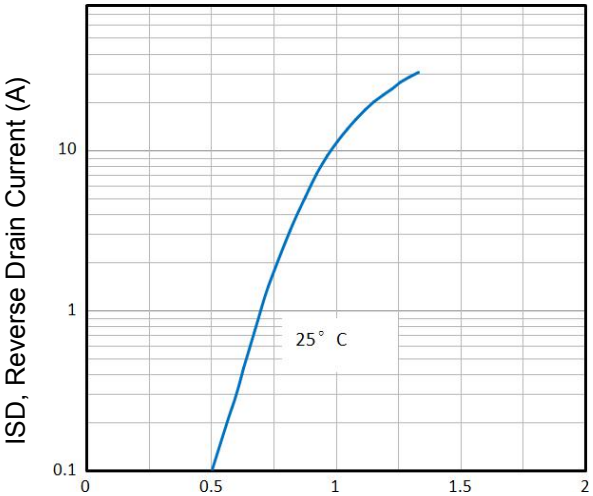
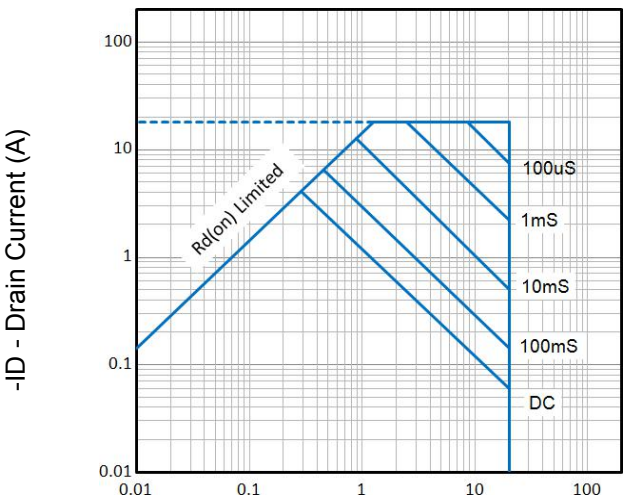


Fig4. Drain -Source Voltage vs Gate -Source Voltage





Typical Characteristics

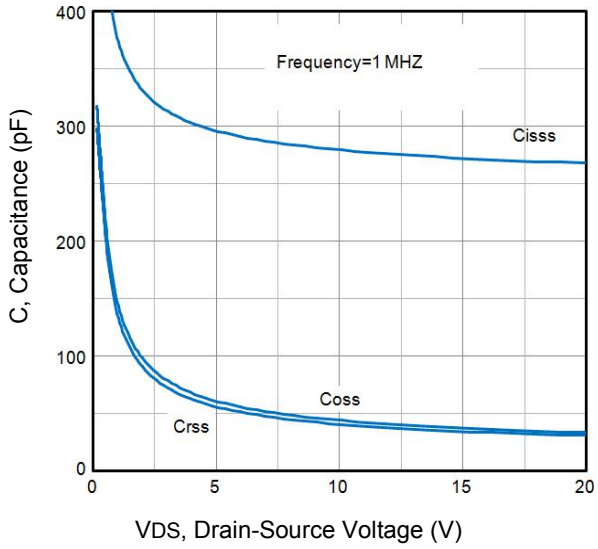


Fig7. Typical Capacitance Vs. Drain-Source Voltage

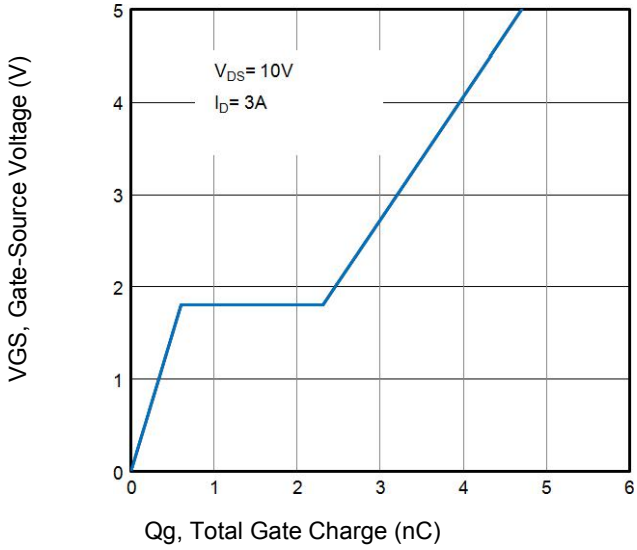


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

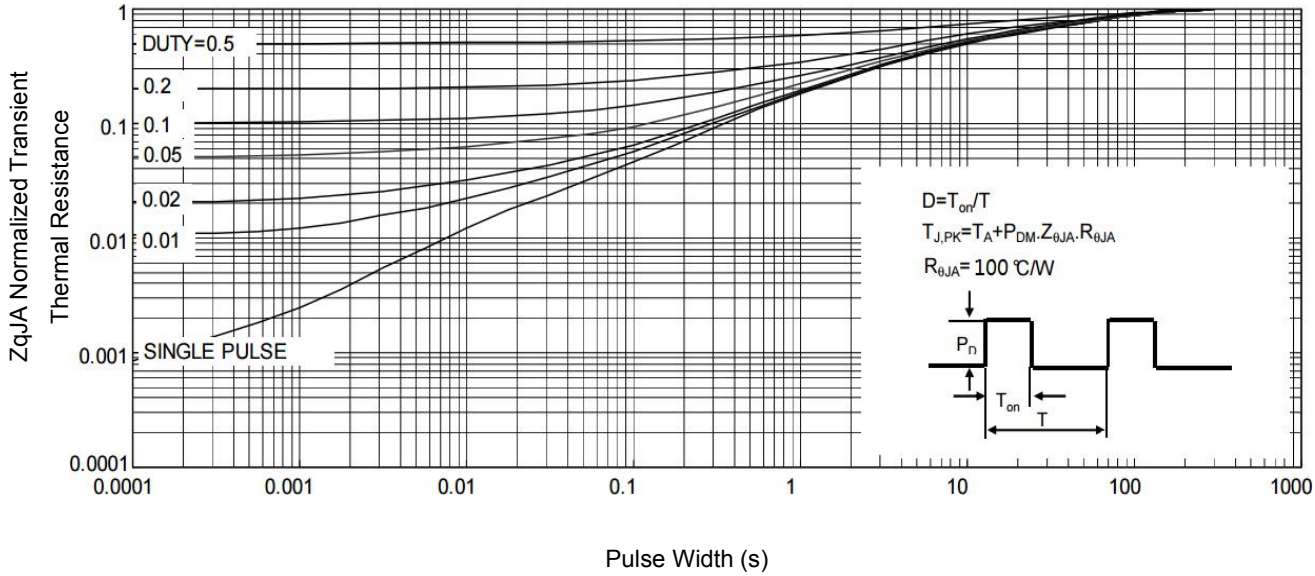


Fig9. Normalized Maximum Transient Thermal Impedance

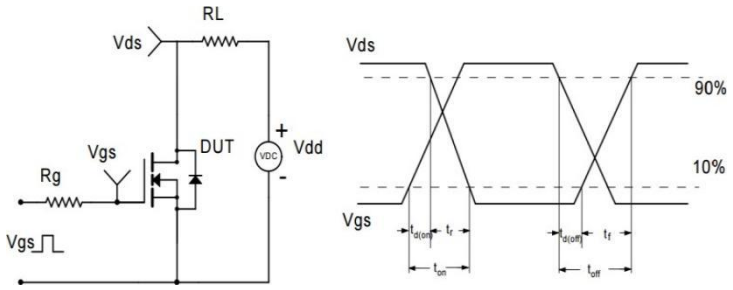
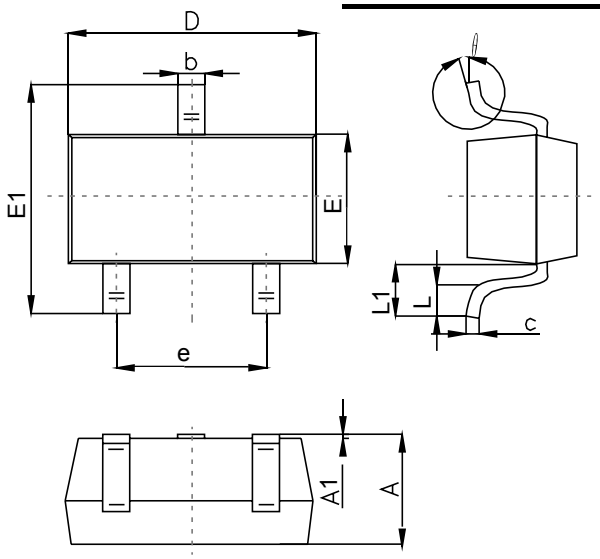


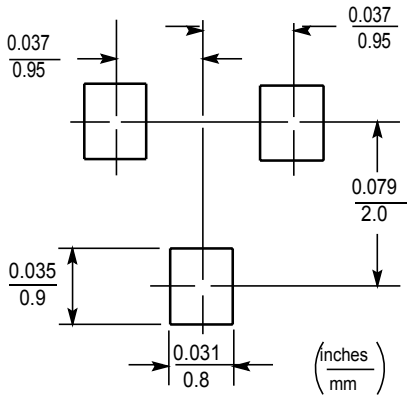
Fig10. Switching Time Test Circuit and waveforms

SOT-23 Package Outline Dimensions



Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A	1.00		1.40
A1			0.10
b	0.35		0.50
c	0.10		0.20
D	2.70	2.90	3.10
E	1.40		1.60
E1	2.4		2.80
e		1.90	
L	0.10		0.30
L1	0.4		
θ	0°		10°

Suggested Pad Layout



Note:
1. Controlling dimension:in/millimeters.
2. General tolerance: ±0.05mm.
3. The pad layout is for reference purposes only.