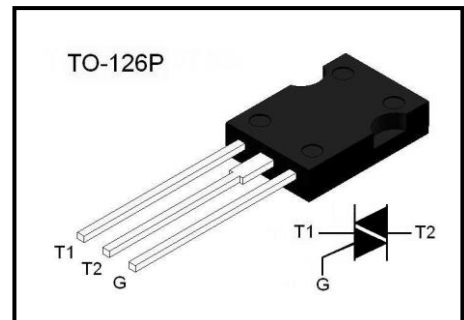


General description

Glass passivated triacs in a plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance.

Typical applications

include motor control, industrial and domestic lighting, heating and static switching.



Absolute Maximum Rating (Ta=25°C)

Limiting values in accordance with the Absolute Maximum System

Parameter	Symbol	Conditions		Ratings	Unit
Repetitive peak off-state voltages	$V_{RRM,DRM}$			500 600 800	V
On-State RMS Current	$I_T(RMS)$	full sine wave; $T_{mb} \leq 108\text{ }^{\circ}\text{C}$		2	A
Non-repetitive peak on-state current	I_{TSM}	full sine wave; $T_j = 25\text{ }^{\circ}\text{C}$ prior to surge	$t = 20\text{ ms}$	20	A
			$t = 16.7\text{ ms}$	22	
I^2t for fusing	I^2t	$t = 10\text{ ms}$		0.5	A^2s
Repetitive rate of rise of on-state current after triggering	dI_T/dt	$I_{TM} = 3\text{ A}; I_G = 0.2\text{ A};$ $dI_G/dt = 0.2\text{ A}/\mu\text{s}$	T2+ G+	50	$\text{A}/\mu\text{s}$
			T2+ G-	50	
			T2- G-	50	
			T2- G+	3	
Peak gate current	I_{GM}			2	A
Peak Gate Voltage	V_{GM}			5	V
Peak gate power	P_{GM}			5	W
Average gate power	$P_{G(AV)}$	over any 20 ms period		0.5	W
Operating junction temperature	T_j			-40 ~ 125	$^{\circ}\text{C}$
Storage Temperature	T_{stg}			-40 ~ 150	$^{\circ}\text{C}$

Thermal Resistances

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Thermal resistance junction to solder point	$R_{th\text{ j-sp}}$	full or half cycle	-		15	$^{\circ}\text{C}/\text{W}$
Thermal resistance junction to ambient	$R_{th\text{ j-a}}$	pcb mounted; minimum footprint pcb mounted;	-	156 70		$^{\circ}\text{C}/\text{W}$

Electrical Characteristics ($T_j=25^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Peak Repetitive Blocking Current	$I_{\text{DRM}}, I_{\text{RRM}}$	$V_{\text{D}} = \text{Rated } V_{\text{DRM}}, V_{\text{RRM}}$ Gate open			10 0.5	μA mA
Gate trigger current	I_{GT}	$V_{\text{D}} = 12 \text{ V}, I_{\text{GT}} = 0.1 \text{ A}$	T2+ G+		10	mA
			T2+ G-		10	
			T2- G-		10	
			T2- G+		15	
Gate trigger voltage	V_{GT}	$V_{\text{D}} = 12 \text{ V}, I_{\text{GT}} = 0.1 \text{ A}$			1.5	V
Latching current	I_{L}	$V_{\text{D}} = 12 \text{ V}, I_{\text{GT}} = 0.1 \text{ A}$	T2+ G+		10	mA
			T2+ G-		10	
			T2- G-		10	
			T2- G+		20	
Holding current	I_{H}	$V_{\text{D}} = 12 \text{ V}, I_{\text{GT}} = 0.1 \text{ A}$			10	mA
On-state voltage	V_{TM}	$I_{\text{T}} = 3 \text{ A}$			1.5	V

Dynamic Characteristics $T_j = 25^{\circ}\text{C}$ unless otherwise stated

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Critical Rate-of-Rise of Commutation Voltage	dV_{D}/dt	$V_{\text{D}} = 67\% V_{\text{DRM(max)}}$, $T_j = 125^{\circ}\text{C}$ exponential waveform; gate open		5.0		V/ μs
Critical Rate of Rise of Off-State Voltage	dV_{com}/dt	$V_{\text{D}} = \text{Rated } V_{\text{DRM}}$, $T_j = 95^{\circ}\text{C}$ $I_{\text{T(RMS)}} = 1 \text{ A}$, $dI_{\text{com}}/dt = 1.8 \text{ A/ms}$ Gate open circuit		50		V/ μs
Turn-On Time	t_{gt}	$V_{\text{D}} = \text{Rated } V_{\text{DRM}}$, $dI_{\text{G}}/dt = 5 \text{ A}/\mu\text{s}$ $I_{\text{TM}} = 1.5 \text{ A}$, $I_{\text{G}} = 0.15 \text{ A}$		2.0		μs

Typical Characteristics

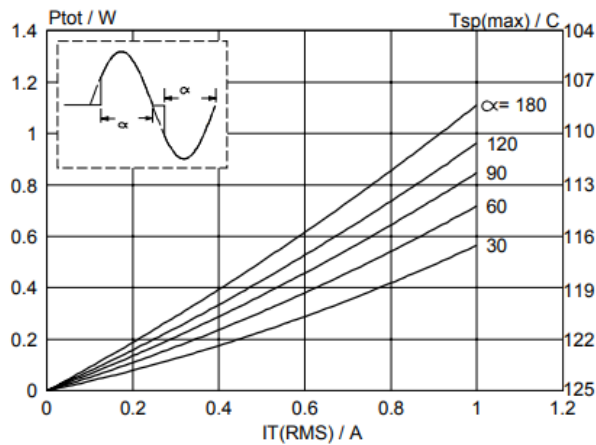


Fig.1. Maximum on-state dissipation, P_{tot} , versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

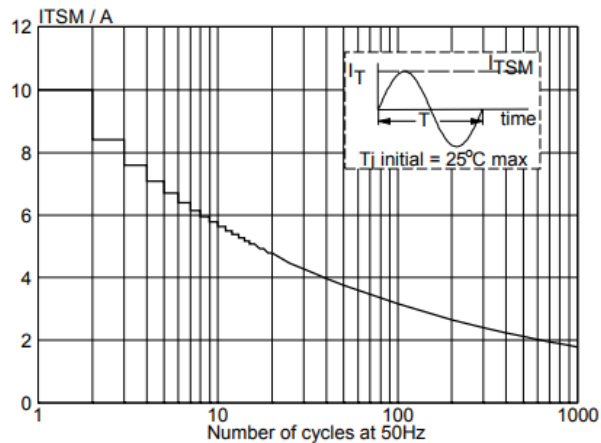


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus number of cycles, for sinusoidal currents, $f = 50$ Hz.

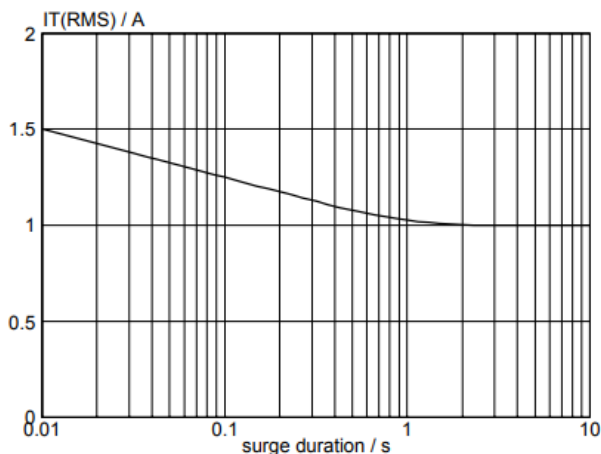


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, $f = 50$ Hz; $T_{sp} \leq 108^\circ\text{C}$.

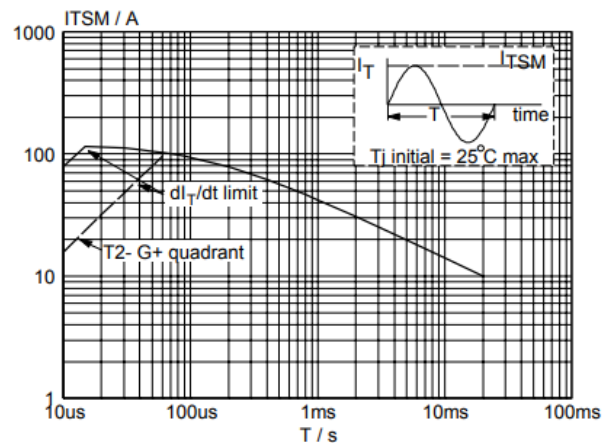


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus pulse width t_p , for sinusoidal currents, $t_p \leq 20$ ms.

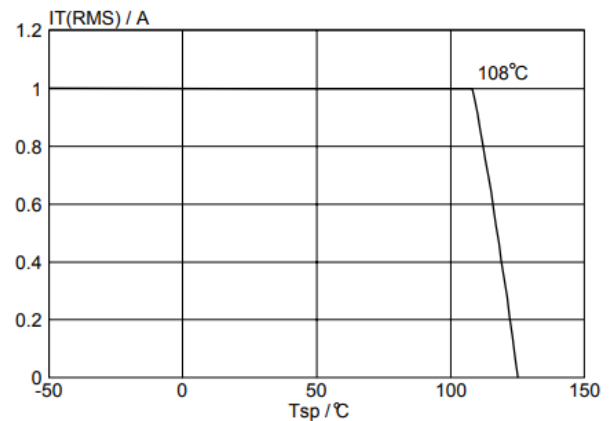


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus solder point temperature T_{sp} .

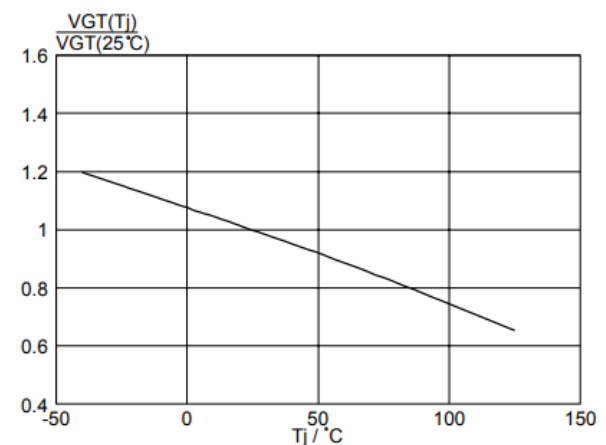


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25^\circ\text{C})$, versus junction temperature T_j .

Typical Characteristics

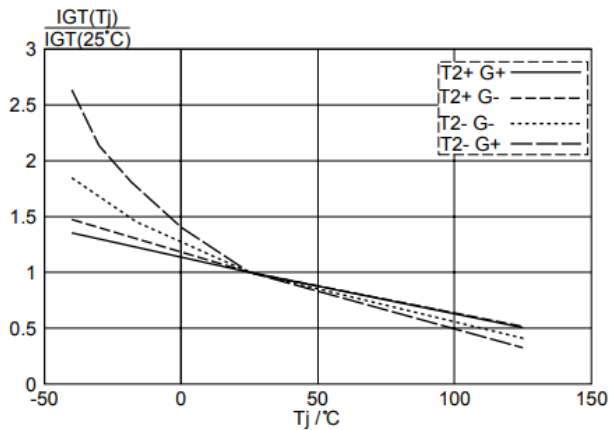


Fig.7. Normalised gate trigger current $I_{GT}(T_j) / I_{GT}(25^\circ\text{C})$, versus junction temperature T_j .

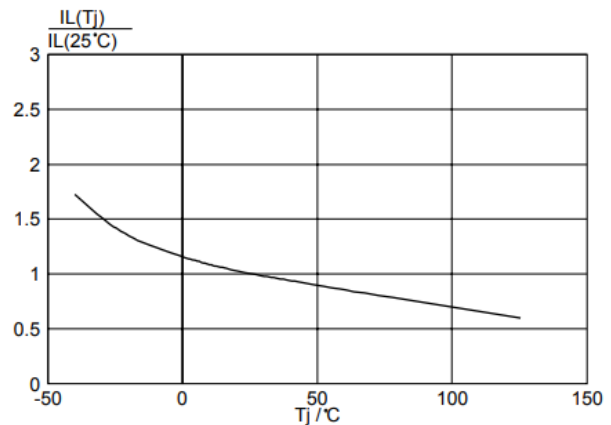


Fig.8. Normalised latching current $I_L(T_j) / I_L(25^\circ\text{C})$, versus junction temperature T_j .

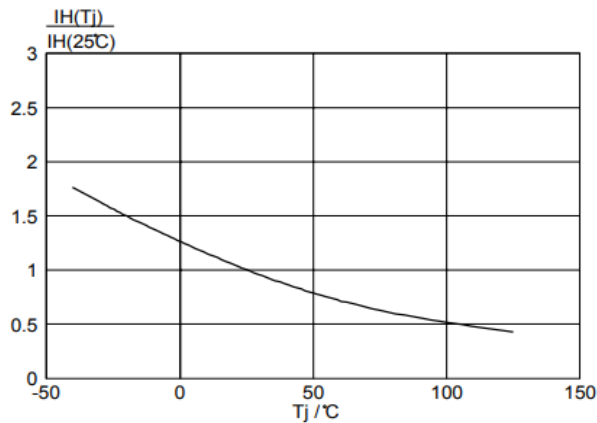


Fig.9. Normalised holding current $I_H(T_j) / I_H(25^\circ\text{C})$, versus junction temperature T_j .

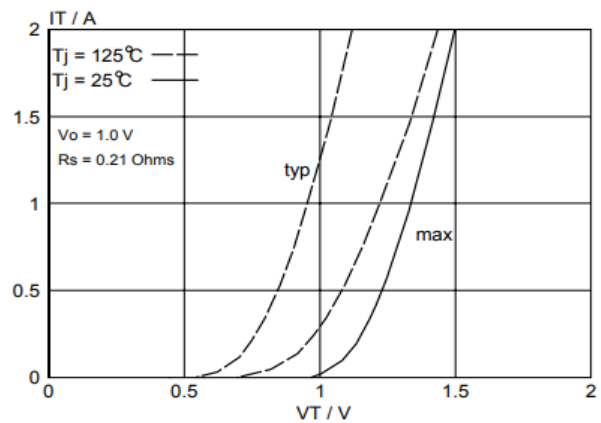


Fig.10. Typical and maximum on-state characteristic.

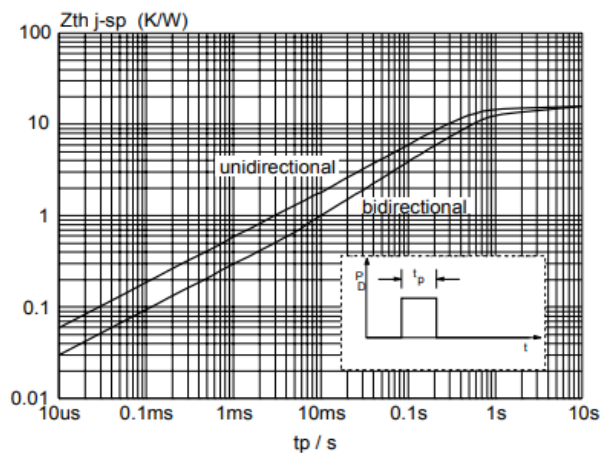


Fig.11. Transient thermal impedance $Z_{th j-sp}$, versus pulse width t_p .

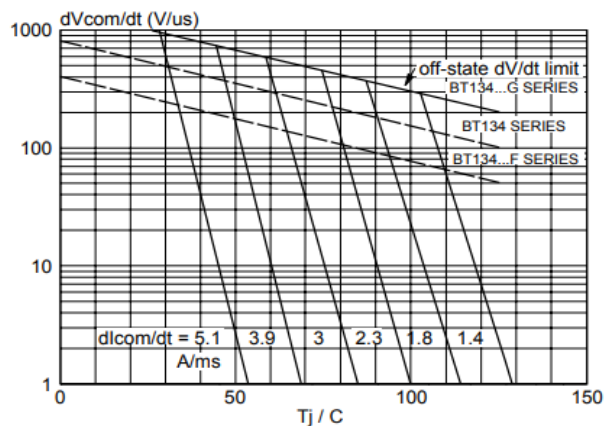


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt . The triac should commute when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt .

Package Dimensions

Dim	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	2.40	2.80	0.094	0.110
A1	1.00	1.40	0.039	0.055
b	0.66	0.86	0.026	0.034
b1	1.17	1.37	0.046	0.054
c	0.40	0.60	0.016	0.024
D	7.30	7.70	0.287	0.303
E	10.60	11.00	0.417	0.433
e	2.25	2.33	0.089	0.092
e1	4.50	4.66	0.177	0.183
L	14.00	15.00	0.551	0.591
L1	1.90	2.50	0.075	0.098
Φ	3.10	3.30	0.122	0.130