Transition-Mode PFC and Quasi-Resonant Current Mode PWM Controller

REV. 00-LITEON

General Description

The LD7798CG features transition mode Power Factor Correction (PFC) voltage mode controller with THDi optimizer and Quasi-Resonant (QR) current mode controller for high power application.

With intelligent PFC on/off, zero current detection (ZCD) without aux-winding and frequency limitation mechanism to achieve better performance.

The IC also integrates several functions, such as brown-in/out protection, Over Load Protection (OLP), Over Temperature Protection (OTP), PFC Bulk Over Voltage Protection (PFCOVP), Output Over Voltage Protection (FBAUXOVP), Over Current Protection (OCP) with high / low line compensation and a protection pin for customized control. Therefore it can protect the system from damage due to occasional failure.

The LD7798CG is available in a SOP-16 package.

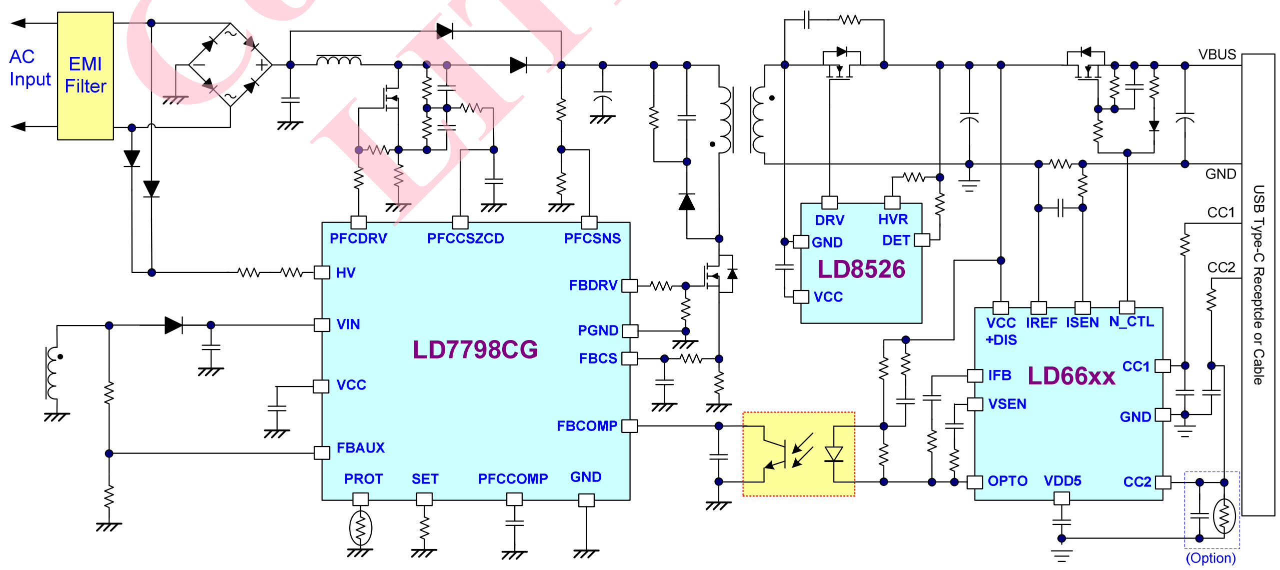
Features

- Integrated Boost PFC and QR Flyback Controller
- Voltage mode transition operation for PFC
- Current mode quasi-resonant operation for Flyback
- 180V VIN max rating for wide V_{OUT} range application
- Smart stabilization system and high efficiency for USB-PD Application
- Brown in/out protection and X-cap discharge function
- Internal soft start function and PFC on/off control
- OVP (Over voltage protection)
- OCP (Cycle by cycle current limiting)
- Internal OTP function and External protection pin
- 550/-1000mA PFC Gate Source/Sink Capability
- 350/-1000mA Flyback Gate Source/Sink Capability

Applications

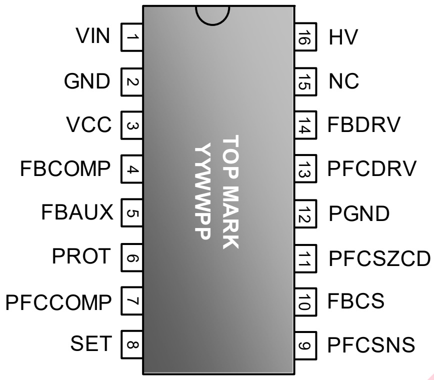
- Power Delivery (PD) Application
- Power Adapter

Typical Application



Pin Configuration

SOP-16 (TOP VIEW)



YY : Year code
WW : Week code
PP : Production code

Ordering Information

Part number	Package	Top Mark	Shipping
LD7798CGGS1	SOP-16	LD7798CGGS1	2500 /tape & reel

The LD7798CGS1 are RoHS compliant / green packaged.

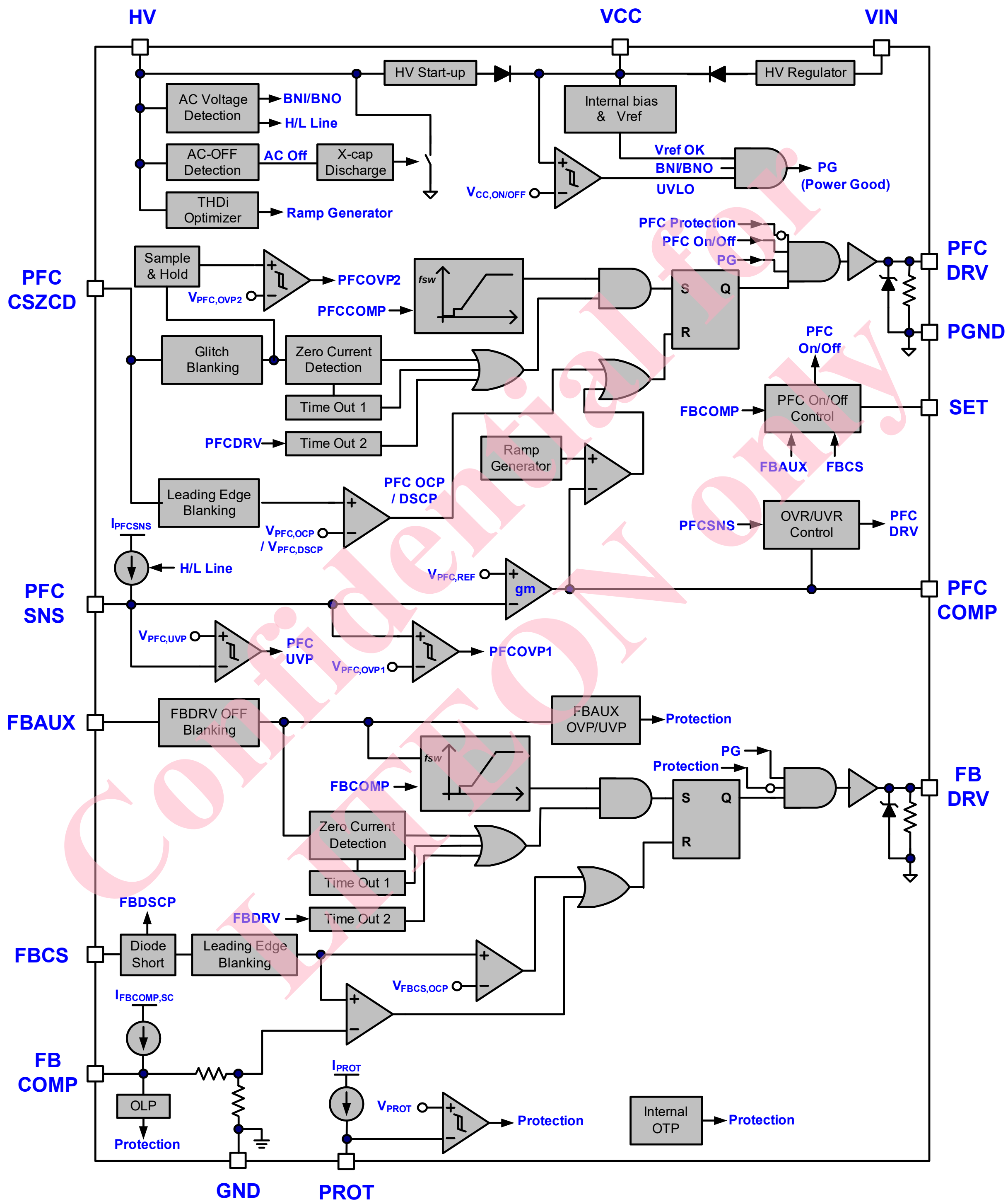
Protection Mode

Part number	Frequency Limitation	VCC OVP FBAUX OVP	FBCOMP OLP FBAUX UVP	PFC & Flyback OCP	PROT (pin 6)	Internal OTP	FBCS DSCP	FBCS Short FBAUX Open
LD7798CG	400kHz (PFC) 130kHz (Flyback)	Auto recovery	Auto recovery	Cycle by cycle	Auto recovery	Auto recovery	Auto recovery	Auto recovery

Pin Descriptions

Pin	NAME	FUNCTION
1	VIN	Input of an internal high voltage regulator
2	GND	Signal ground.
3	VCC	Supply IC voltage pin. Output of an internal high voltage regulator
4	FBCOMP	Voltage feedback compensation of flyback stage. Connect a photo-coupler as close as to the control loop and achieve the output voltage regulation.
5	FBAUX	Zero current detection and output voltage monitoring of flyback.
6	PROT	External protection pin.
7	PFCCOMP	Output of the error amplifier for PFC voltage loop compensation.
8	SET	Preset and control the PFC On/Off operation.
9	PFCSNS	Voltage feedback sensing for PFC output voltage
10	FBCS	Connect it to sense the flyback MOSFET current.
11	PFCCSZCD	Over current protection and zero current detection of PFC.
12	PGND	Power Ground. The path of PFC and flyback MOS driving.
13	PFCDRV	Gate drive output to drive the external MOSFET for PFC.
14	FBDRV	Gate drive output to drive the external MOSFET for flyback.
15	NC	No Connection. High voltage safety spacer.
16	HV	Connect this pin to Line/Neutral of AC voltage through diodes and resistors to provide the startup current for the controller. When VCC voltage increases to above UVLO(on), this HV loop will be turned off to reduce the power loss over the startup circuit. HV pin also detects the AC voltage & cycles, providing brown in/out, high/low line detection and X-cap discharge functions.

Block Diagram



Absolute Maximum Ratings

VIN	-0.3V ~ 180V
VCC	-0.3V ~ 32V
HV	-0.3V ~ 650V
FBCOMP, PFCCOMP, FBCS, PFCSNS, FBAUX, PFCCSZCD, PROT, SET	-0.3V ~ 6V
FBDRV, PFCDRV	-0.3V ~ 20V
Maximum Junction Temperature	-40°C ~ 150°C[1]
Storage Temperature Range	-65°C ~ 150°C
Power Dissipation (SOP-16, at Ambient Temperature = 85°C)	363mW
Package Thermal Resistance (SOP-16, θ_{JA})	110°C/W
Package Thermal Resistance (SOP-16, θ_{JC})	36°C/W
Lead Temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (Pin 1, 16)	1.0kV
ESD Voltage Protection, Human Body Model (Pin 3~11, 13~14)	2.5kV

Note1: For system application, refer to recommended operating conditions.

Caution:

Stresses beyond the ratings specified in "absolute maximum ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
AC Input Voltage	90	264	V_{rms}
AC Input Line Frequency	47	63	Hz
HV Pin Capacitance	--	220	pF
VIN Pin Capacitance	10	--	μF
Current from VIN to VCC	--	12	mA
VCC Pin Capacitance	10	--	μF
FBCOMP, PFCSNS Pin Capacitance	0.47	10	nF
PROT, SET Pin Capacitor	--	10	nF
PFC MOS Gate to Source Resistor	10k	82k	Ω
FBAUX Source Current	--	1	mA

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF~0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible.
2. Connecting a capacitor to PFCCOMP & FBCOMP pin is also essential to filter out the undesired switching noise for stable operation.
3. Place the small signal components closed to IC pin as possible.
4. The recommended operating conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Leadtrend does not recommend exceeding them or designing to absolute maximum ratings.
5. In selection of these external components, make sure that their values including temperature & tolerance characteristics are satisfied with the recommended ranges.

Electrical Characteristics

(VCC=20V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
High-Voltage Supply (HV Pin)						
High-Voltage Current Source for VCC Startup	VCC = 0V, V_{HV} = 80V	I_{HV0}	0.4	1.2	2.0	mA
	*, VCC = 5V, V_{HV} = 80V	I_{HV1}	1.0	3.0	6.0	mA
	VCC = V_{CC_ON} -1V, V_{HV} = 80V	I_{HV2}	1.5	3.0	5.5	mA
Off-State Leakage Current	UVLO(on), V_{HV} = 650V	$I_{HV,OFF}$	0		32	μA
X-cap discharge current	*	$I_{HV,XCAP}$	1	3	6	mA
X-cap discharge Time	*	T_{XCAP}	220	250	280	ms
Line Voltage Detection (HV Pin)						
Brown-in DC Level		$V_{HV,BNI}$	105	110	115	V
Brown-in De-bounce Time	*	$T_{D,BNI}$	565	640	715	μs
Brown-out DC Level		$V_{HV,BNO}$	97	102	107	V
Brown-out De-bounce Time	*	$T_{D,BNO}$	54	61	68	ms
High Line DC Level		$V_{HV,HL}$	207	219	231	V
High Line De-bounce Time	*	$T_{D,HL}$	1.01	1.28	1.54	ms
Low Line DC Level		$V_{HV,LL}$	201.0	212.5	224.0	V
Low Line De-bounce Time	*	$T_{D,LL}$	54	61	68	ms
Supply Voltage (VCC Pin)						
UVLO (on)		$V_{CC,ON}$	20.0	21.3	22.5	V
VCC Brown-in Enable Level	UVLO (on)	$V_{CC,BNI}$	16.7	18.0	19.3	V
UVLO (off)		$V_{CC,OFF}$	7.5	8.0	8.5	V
Power Down Reset Level	*	$V_{CC,PDR}$	6	7	8	V
Holding Current	*, VCC < UVLO (on)	$I_{VCC,ST0}$	20	35	50	μA
	*, UVLO (on) is Ready, Brown-in is Not Ready	$I_{VCC,ST1}$		300	500	μA
	*, Auto Recovery Protection	$I_{VCC,AUTO}$	600	800	1000	μA
Operating Current (C_{PFCDRV}=1nF, C_{FBDRV}=1nF)	*, PFCCOMP=FBCOMP=0V	$I_{VCC,0}$	0.6	0.8	1.1	mA
	*, PFCCOMP=FBCOMP=3V	$I_{VCC,3}$		6.5	10	mA
VCC OVP Level		$V_{CC,OVP}$	28.5	30.0	31.5	V
VCC OVP De-bounce Time	*	$T_{D,VCCOVP}$	70	80	90	μs
VCC Regulated Voltage	VIN=50V	$V_{CC,REG}$	13.0	16.5	20.0	V

*: Guaranteed by design.

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
External Protection (PROT Pin)						
Source Current		I_{PROT}	75	80	85	μA
Turn-On Trip Level		$V_{PROT,ON}$	1.30	1.35	1.40	V
Turn-Off Trip Level		$V_{PROT,OFF}$	1.20	1.25	1.30	V
Turn-Off Resistance	$V_{PROT,OFF}$ / I_{PROT}	$R_{PROT,OFF}$	14.35	15.60	16.85	kΩ
Protection De-bounce time	*, V_{PROT} High to Low	$T_{D,PROT}$	422	480	538	μs
On Chip Thermal Shutdown (Internal OTP)						
OTP Level	*	T_{OTP}	125	140	150	°C
OTP Hysteresis	*	$T_{OTP,HYST}$	25	40	55	°C
PFC ON/OFF Control (SET Pin)						
Preset Current of PFCON		$I_{PFCON,SET}$	22	25	28	μA
PFC On De-bounce Time	*, V_{FBCOMP} < 2.7V	$T_{D,PFCON}$	4	5	6	ms
PFC Off De-bounce Time	*, $R_{SET} \leq 91k\Omega$	$T_{D,PFCOFF}$	8.5	10	11.5	sec
PFC Output Voltage Sensing (PFCSNS pin)						
Feedback Reference Voltage		$V_{PFC,REF}$	2.460	2.500	2.540	V
PFCSNS OVP1 Level	Low Line	$V_{PFC,OVP1,LL}$	2.690	2.750	2.810	V
	High Line, Normal Mode	$V_{PFC,OVP1,HL}$	2.620	2.675	2.730	V
	*, High Line, Burst Mode	$V_{PFC,OVP1,HLBM}$	2.515	2.575	2.635	V
PFCSNS OVP1 Reset	*	$V_{PFC,OVP1RST}$	2.490	2.550	2.610	V
Source Current of PFCSNS	Low Line	$I_{PFCSNS,LL}$	9	10	11	μA
	*, High Line	$I_{PFCSNS,HL}$	0		0.2	μA
PFC UVP Trip Level		$V_{PFC,UVP}$	0.15	0.20	0.25	V
PFC UVP Hysteresis Level	*	$V_{PFC,UVPHYST}$	0.06	0.10	0.14	V
Pull Down Sink Current	*	$I_{PFCSNS,SINK}$	0		0.2	μA
PFC Error Amplifier (PFCCOMP Pin)						
Transconductance	*, PFCSNS=$V_{PFC,REF}$ - 20mV	gm_{PFC}	9	15	21	μmho
Output High Clamp Voltage	PFCSNS = V_{REF} - 0.1V	$V_{PFCOMP,MAX}$	4.8	5.0	5.2	V
PFC Enable Level	*, PFCCOMP Rising	$V_{PFCCOMP,ON}$	0.95	1.00	1.05	V
PFC Disable Level	*, PFCCOMP Falling	$V_{PFCCOMP,OFF}$	0.90	0.95	1.00	V
PFC Max. On-Time (w/o THD Compensation)	Low Line	$T_{ON,PFC,MAX,LL}$	19	21	23	μs
	High Line	$T_{ON,PFC,MAX,HL}$	7.5	8.3	9.1	μs
PFC Maximum Frequency 1	$V_{PFCCOMP}$=3V	$f_{PFC,MAX,H}$	360	400	440	kHz
PFC Maximum Frequency 2		$f_{PFC,MAX,G}$	25	30	35	kHz

*: Guaranteed by design.

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
PFC Current Sensing (PFCCSZCD Pin)						
Cycle by Cycle Current Limit	Low Line	$V_{PFCOCP,LL}$	0.58	0.63	0.68	V
	High Line	$V_{PFCOCP,HL}$	0.48	0.53	0.58	V
Leading Edge Blanking Time		$T_{LEB,PFC}$	450	550	650	ns
PFC Zero Current Detection (PFCCSZCD Pin)						
PFC Minimum Off-Time		$T_{OFF,PFC,MIN}$	1.5	1.8	2.1	μs
PFC ZCD Time Out 2	From PFCDRV Rising	$T_{O2,PFC}$	36	42	48	μs
PFCCSZCD OVP2 Level	*	$V_{PFC,OVP2}$	2.610	2.675	2.740	V
PFCCSZCD OVP2 Reset Level	*	$V_{PFC,OVP2RST}$	2.435	2.500	2.565	V
PFCCSZCD OVP2 Time Out	*	$T_{O2,PFCOVP2}$	2.2	2.5	2.8	ms
PFC Gate Drive Output (PFCDRV Pin)						
PFCDRV Output Low Level	*	$V_{PFCDRV,L}$	0		1.5	V
PFCDRV Output High Level	*	$V_{PFCDRV,H}$	9		16	V
Rising Time	*, C_{PFCDRV}=1nF, V_{PFCDRV}=13.5V	$T_{RISE,PFC}$	50	100	150	ns
Falling Time	*, C_{PFCDRV}=1nF, V_{PFCDRV}=13.5V	$T_{FALL,PFC}$	5	20	40	ns
PFC ZCD Delay Setting (PFCDRV Pin)						
Preset Current of PFCDRV	*	$I_{PFCDRV,SET}$	24	30	36	μA
Flyback Compensation (FBCOMP Pin)						
Short Circuit Current		$I_{FBCOMP,SC}$	0.200	0.235	0.270	mA
Open Loop Voltage		$V_{FBCOMP,H}$	5.1	5.4	5.7	V
OLP Trip Level		V_{FBOLP}	4.0	4.2	4.4	V
OLP De-bounce Time	*	$T_{D,FBOLP}$	72	82	92	ms
Maximum Frequency 1	V_{FBCOMP}=2.7V, V_{FBAUX}=4V	$f_{FB,MAX,H}$	120	130	140	kHz
Maximum Frequency 2	V_{FBCOMP}=1.3V, V_{FBAUX}=4V	$f_{FB,MAX,G}$	23	25	27	kHz
Burst Mode Threshold Level	*, Trip Level for FBDRV Stop	$V_{FBCOMP,BM0}$	0.3	0.4	0.5	V
	*, Trip Level for FBDRV Start	$V_{FBCOMP,BM1}$	0.4	0.5	0.6	V

*: Guaranteed by design.

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Flyback Zero Current Detection (FBAUX Pin)						
ZCD Trip Level		$V_{FBAUX,QRL}$	280	350	420	mV
ZCD Reset Level	*	$V_{FBAUX,QRH}$	330	400	470	mV
Minimum Off-Time		$T_{OFF,FB,MIN}$	1.8	2.0	2.2	μs
ZCD Time Out 1	*	$T_{O1,FBAUX}$	2	3	4	μs
ZCD Time Out 2	*	$T_{O2,FBAUX}$	100	150	200	μs
FBAUX Open Detect Current		$I_{FBAUX,OP}$	9	13	17	μA
FBAUX Open Triggered Cycle	*	$T_{C,FBAUX,OP}$	4	6	8	Cycle
FBAUX Open Reset Time	*	$T_{R,FBAUX,OP}$	422	480	538	μs
Flyback Output Voltage Detection (FBAUX Pin)						
FBAUX OVP Trip Level		$V_{FBAUX,OVP}$	5.2	5.4	5.6	V
FBAUX OVP Triggered Cycle	*	$T_{C,FBAUXOVP}$	4	6	8	Cycle
FBAUX OVP Reset Time	*	$T_{R,FBAUXOVP}$	422	480	538	μs
FBAUX UVP Trip Level		$V_{FBAUX,UVP}$	0.14	0.20	0.26	V
Flyback Current Sense (FBCS Pin)						
Flyback Soft Start Time	*	$T_{SS,FB}$	4	5	6	ms
Maximum On Time		$T_{ON,FB,MAX}$	40	45	50	μs
Leading Edge Blanking Time		$T_{LEB,FB}$	205	275	345	ns
Cycle by Cycle Current Limit	Low Line	$V_{FBOCP,LL}$	0.65	0.70	0.75	V
	High Line	$V_{FBOCP,HL}$	0.55	0.60	0.65	V
Min Current Sense Level	After $T_{LEB,FB}$	$V_{FBCS,MIN}$	0.07	0.10	0.13	V
FBCS Short Detect Level	*	$V_{FBCS,SC}$	0.04	0.06	0.08	V
FBCS Short Detect Time	*	$T_{ON,FBCS,SC}$	4	6	8	μs
FBCS Short Triggered Cycle	*	$T_{C,FBCS,SC}$	2	4	6	Cycle
FBCS Short Reset Time	*	$T_{R,FBCS,SC}$	422	480	538	μs
Flyback Gate Drive Output (FBDRV Pin)						
FBDRV Output Low Level	*	$V_{FBDRV,L}$	0		1.5	V
FBDRV Output High Level	*, VCC=17V	$V_{FBDRV,H}$	9		13	V
Rising Time	*, C_{FBDRV}=1nF, V_{FBDRV}=12V	$T_{RISE,FB}$	150	300	450	ns
Falling Time	*, C_{FBDRV}=1nF, V_{FBDRV}=12V	$T_{FALL,FB}$	5	20	40	ns

*: Guaranteed by design

Typical Performance Characteristics

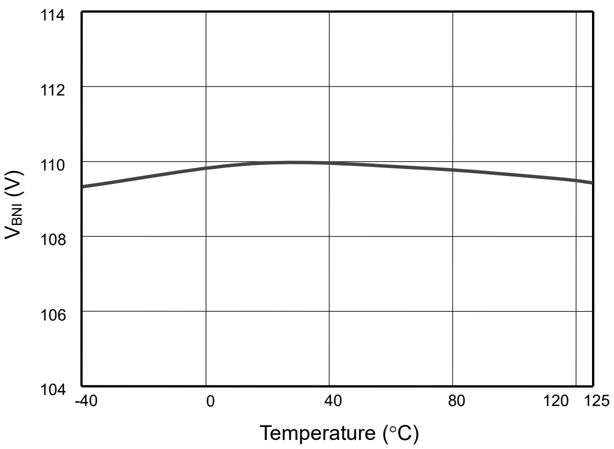


Fig. 1 Brown-in vs. Temperature

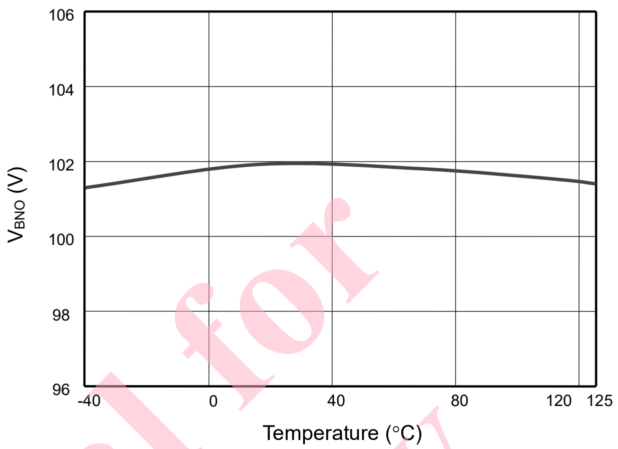


Fig. 2 Brown-out vs. Temperature

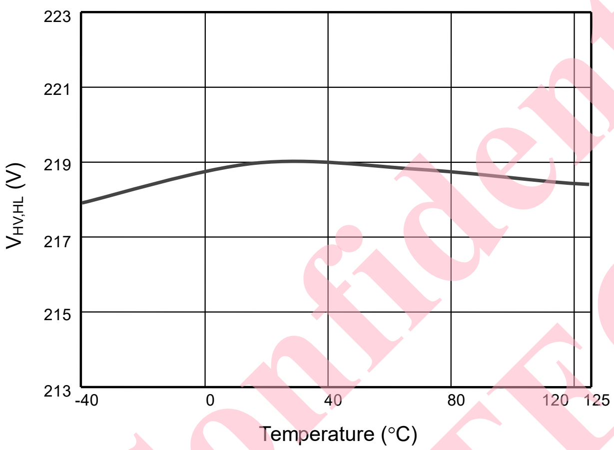


Fig. 3 High Line DC Level vs. Temperature

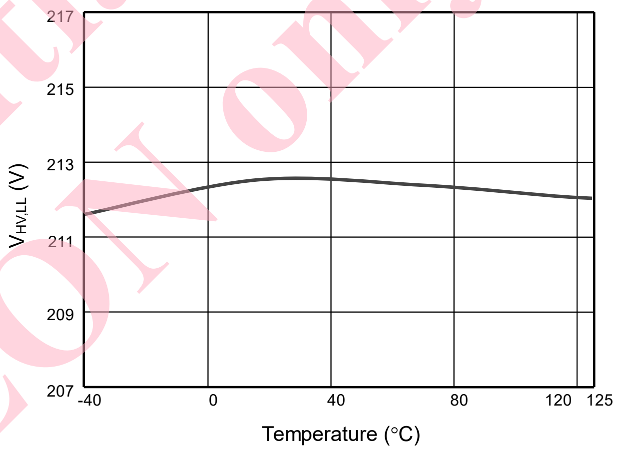


Fig. 4 Low Line DC Level vs. Temperature

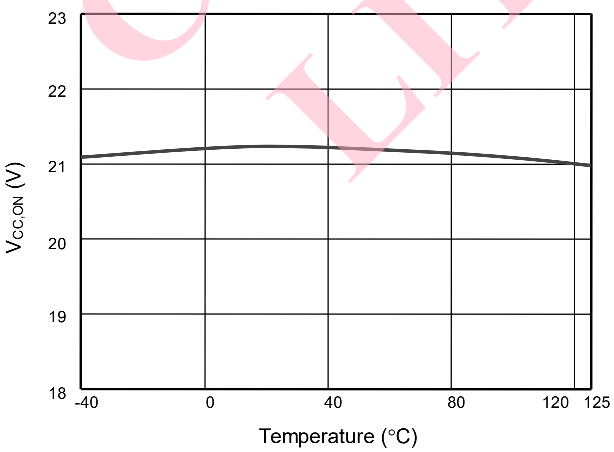


Fig. 5 UVLO (on) vs. Temperature

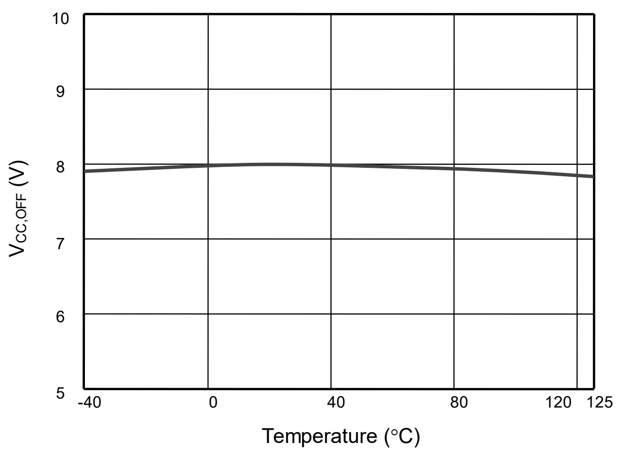


Fig. 6 UVLO (off) vs. Temperature

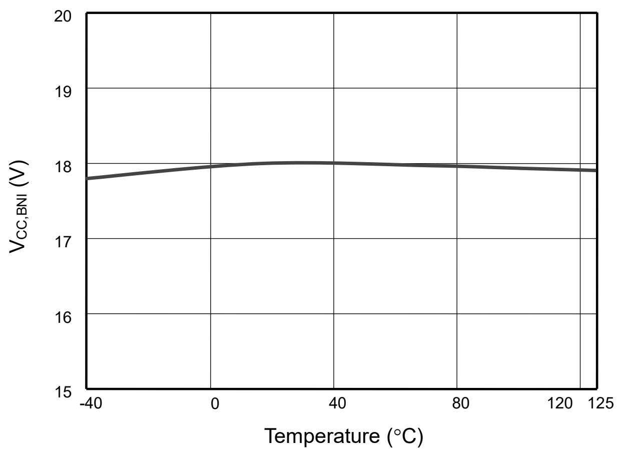


Fig. 7 VCC Brown-in Enable Level vs. Temperature

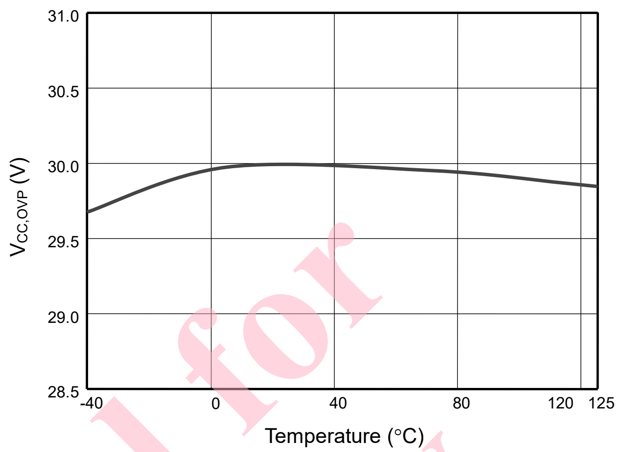


Fig. 8 VCC OVP Level vs. Temperature

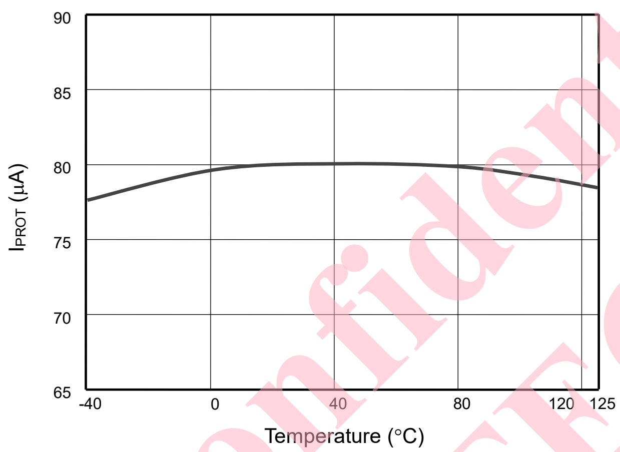


Fig. 9 PROT Source Current vs. Temperature

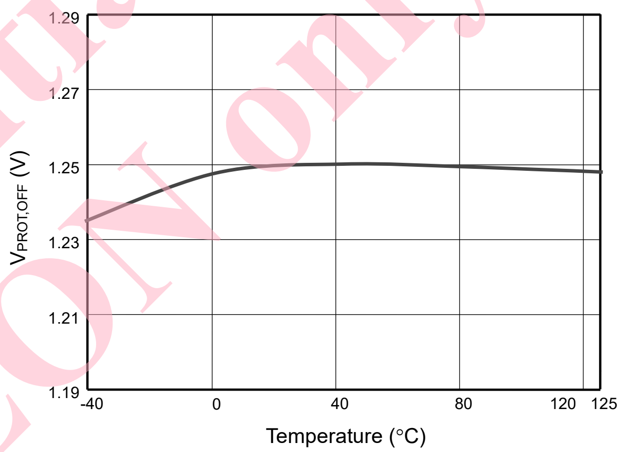


Fig. 10 PROT Turn-Off Trip Level vs. Temperature

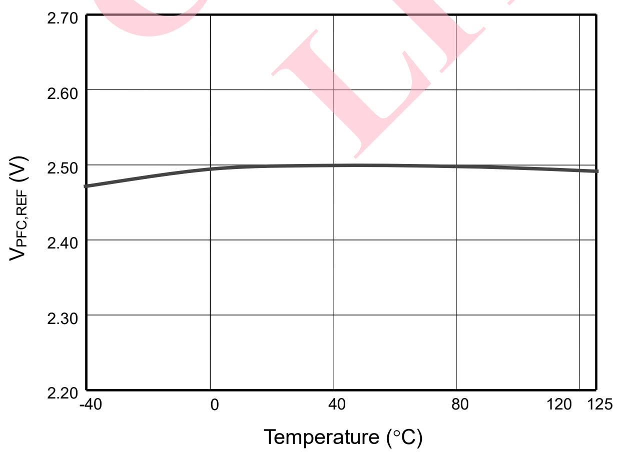


Fig. 11 Feedback Reference Voltage vs. Temperature

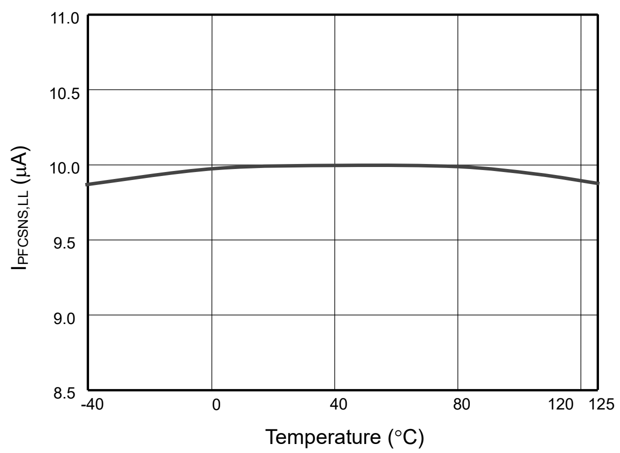


Fig. 12 Source Current of PFCSNS (Low Line) vs. Temperature

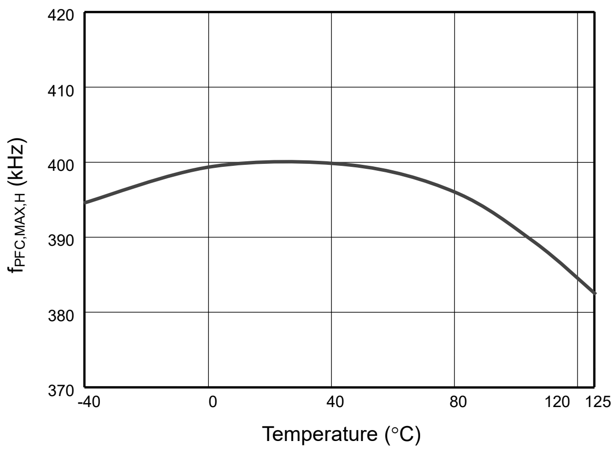


Fig. 13 PFC Max Frequency 1 vs. Temperature

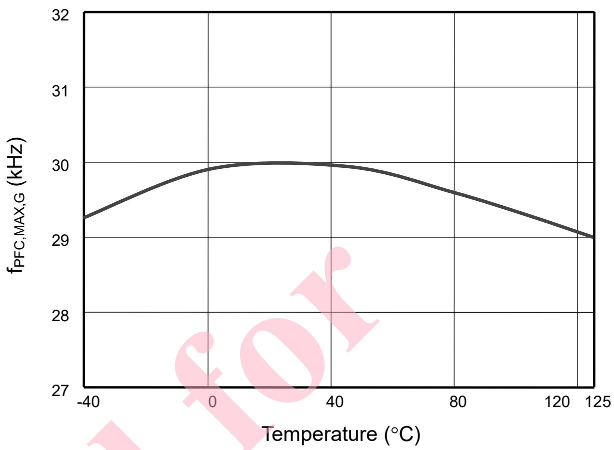


Fig. 14 PFC Max Frequency 2 vs. Temperature

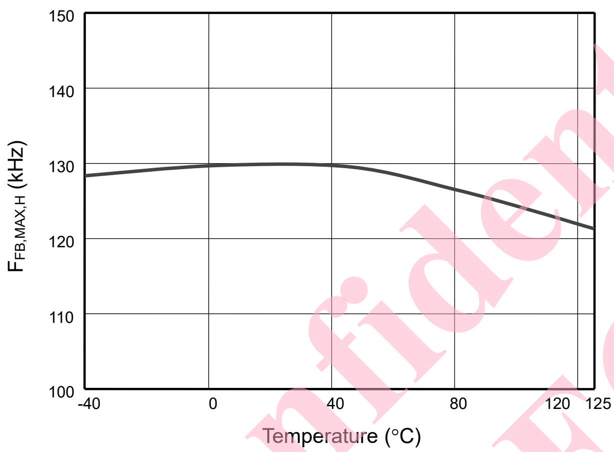


Fig. 15 Flyback Max Frequency 1 vs. Temperature

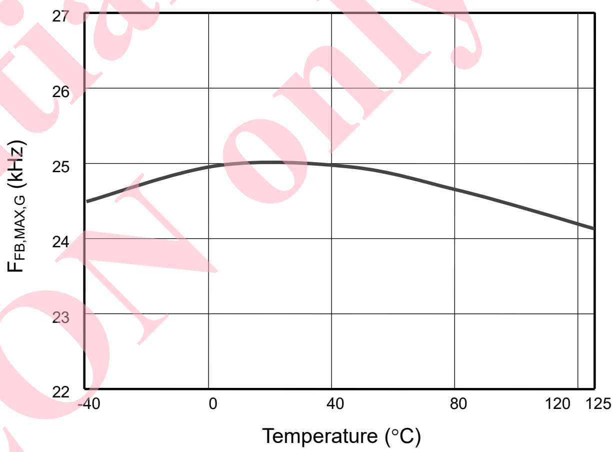


Fig. 16 Flyback Max Frequency 2 vs. Temperature

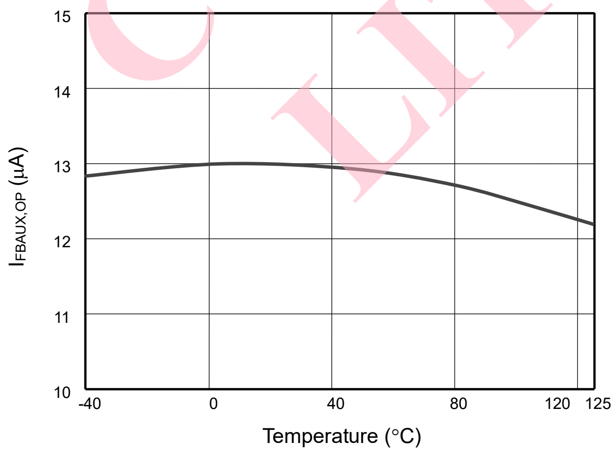


Fig. 17 FBAUX Open Detect Current vs. Temperature

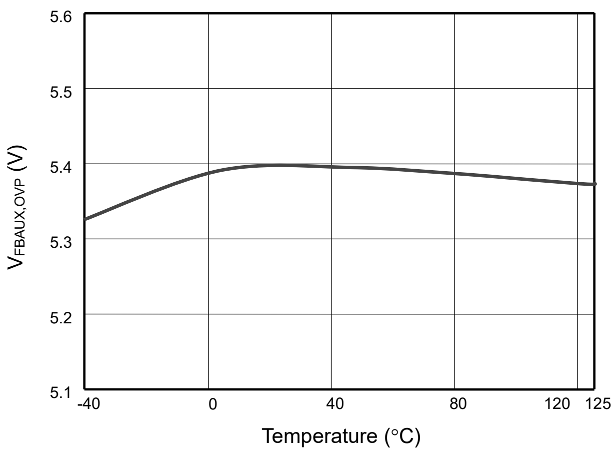


Fig. 18 FBAUX OVP Trip Level vs. Temperature

Application Information

Operation Overview

LD7798CG integrates Boundary Conduction Mode (BCM) voltage mode Power Factor Correction (PFC) and current mode Quasi-Resonant (QR) flyback control in one chip.

To adapt the wide range output voltage in Power Delivery (PD) application, a high voltage (HV) regulator integrates in chip. The max voltage rating on VIN pin is 180V, and voltage regulates to $V_{CC,REG}$ as an output voltage on VCC pin.

PFC stage is operating in Zero Current Switching (ZCS) without aux-winding requirement. Both MOS current information and Zero Current Detection (ZCD) are sensed by pin of PFCCSZCD. To limit the max current of PFC MOS while it is ON, and monitor the ZCD signal in OFF state. Also, there is an intelligent PFC ON/OFF mechanism to improve the transition response of PFC stage. The flyback is in QR operation to achieve high efficiency. The output voltage is monitored by FBAUX pin. The output current is calculated by signals mainly from FBCS and FBAUX pin.

With a single chip controls both PFC and flyback stages, the information between both stages can be well communicated to improve the performance. The detail features are described as below.

Internal HV Startup Current and Under Voltage Lock Out (UVLO)

There is a HV startup current source in chip. Power-up the IC from line and neutral of AC voltage through diodes and resistors. The current is charging VCC capacitor while IC is off. Once VCC voltage rises up to the $V_{CC,ON}$, HV pin will stop sourcing current. This feature minimizes the power loss on the start-up circuit without extension of start-up time.

An UVLO comparator is embedded to detect the voltage on VCC pin and ensure the supply voltage is high enough to power on. The hysteresis is included to prevent from shutdown by the voltage dip during startup.

Brown In/Out Protection (BNI/BNO)

The IC features brown in/out protection on HV pin. A comparator detects AC voltage to prevent damage from ultra-low line operation. While AC voltage is lower than BNO condition, the VCC is keeping hiccups between UVLO On/Off without switching. While AC voltage is high enough, to ensure VCC startup properly, only if VCC>$V_{CC,BNI}$ (18V) can meet BNI condition. The general BNI/BNO thresholds in AC voltage are shown as below:

The example with sinusoidal AC input, 60Hz:

Symbol	Value	Unit
$V_{ac,BNI}$	78	V_{rms}
$V_{ac,BNO}$	72	

High/Low Line Detection

The HV pin detects AC input voltage to improve IC performances. Proper compensations on PFC bulk voltage, OCP and output current monitoring etc. are realized to improvement. The general high/low line thresholds in AC voltage are shown as below:

Takes sinusoidal AC input with 60Hz for example:

Symbol	Value	Unit
$V_{ac,HL}$	160	V_{rms}
$V_{ac,LL}$	150	

PFC Bulk Voltage Setting

The PFC bulk voltage is regulated from PFCSNS pin. With a proper resistor divider feedbacks to PFCSNS pin in $V_{PFC,REF}$ (2.5V). A voltage to current amplifier regulates the control loop. There is compensation current in low line, sourcing current to the feedback resistors. It will change the control loop and regulate a lower bulk voltage in this condition. The calculation is show as below. Please refer to Fig. 19 for more detail.

$$V_{BULK,HL} \cong V_{PFC,REF} \cdot \left(1+\frac{R_{PFCSNS,H}}{R_{PFCSNS,L}}\right)$$

$$V_{BULK,LL} \cong V_{BULK,HL} - \left(I_{PFCSNS,LL} \cdot R_{PFCSNS,H}\right)$$

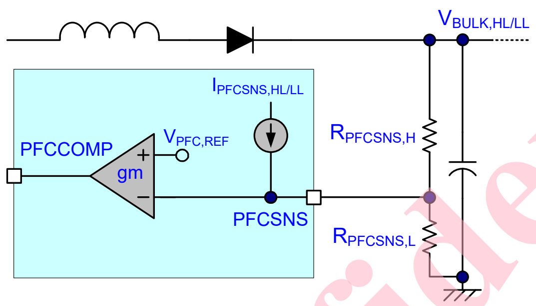


Fig. 19

Furthermore, once the feedback voltage on this pin is higher than $V_{PFC,OVP1}$, the PFC OVP1 will be triggered. The PFCDRV stop switching to avoid over voltage damage, but the flyback stage is still working.

PFC Current Sense and ZCD Detection

Different from detecting ZCD signal by aux-winding, this chip integrates current sensing and ZCD detecting into one single pin. From Fig.20, the current through the PFC MOS is observed when it is on. A generally cycle by cycle over current limit is obtained. Additionally, if $V_{PFCCSZCD}$ > 1.5V is detected after $T_{LEB,PFC}$, it is considered as diode short condition, the PFC is in time out mode (2.3ms). When PFC MOS is off and the inductor current starts discharging, a comparator is monitoring the drain voltage, which is also close to the bulk voltage, through voltage divider. If the feedback sensing result is over $V_{PFC,OVP2}$, PFC OVP2 will be triggered and PFCDRV will switch into time out mode. While the inductor current discharges to none, the drain voltage is falling obviously. IC detects this drain voltage variation as the ZCD signal. To avoid the spike ringing, a 1.8μs period is blanked after the PFCDRV pull low. Then IC starts to detect the zero current point by knee point detection technics. When the inductor current reaches zero, the PFC inductor starts resonant with the parasitic capacitors and $V_{DS,PFC}$ starts to fall. This falling edge is detected as the zero current point.

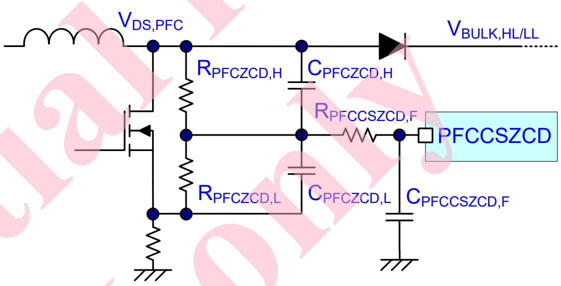


Fig. 20

To guarantee the operating quality, a proper design and characteristic on resistors and capacitors from drain to ground is strongly requested. Furthermore, considering to the temperature variation, the capacitor type of C0G or NP0 on $C_{PFCZCD,H}$, $C_{PFCZCD,L}$ and $C_{PFCCSZCD,F}$ is strongly recommended.

The PFC ZCD delay can be preset by the resistance from PFCDRV pin to ground. A 30μA current is sourcing out to detect in the first 4ms after brown in is ready. Typically, the resistor on PFC MOS gate to source is the dominant. The recommended resistances are shown as below.

$R_{PFCDRV-GND}$	PFC ZCD Delay	
10kΩ	#1	300ns
33kΩ	#2	350ns
62kΩ	#3	400ns
Note: $R_{GS,PFC}$>100kΩ is NOT recommended		

PFC Under Voltage Protection (PFCUVP)

To avoid PFC bulk voltage out of control while PFCSNS pin and the divider resisters are in open / short conditions. Once the sensing voltage on PFCSNS is lower than $V_{PFC,UVP}$, PFCDRV and FBDRV stop switching and IC goes into protection mode.

There is a case which is different from others. Refer to Fig. 19. When $R_{PFCSNS,H}$ is open in low line after UVLO on, the voltage drop by $I_{PFCSNS,LL}$ x $R_{PFCSNS,L}$ may cause the V_{PFCSNS} not low enough to trigger PFCUVP. In this condition, the bulk voltage keeps rising until PFCOVP2 is triggered. If PFCOVP2 is detected but V_{PFCSNS} is relatively low, IC will turn off $I_{PFCSNS,LL}$ source current and lead this case into PFCUVP protection.

PFC Frequency Limitation

To avoid the switching frequency goes too high while the sinusoidal AC voltage is around 0°/180° phase, the IC limits maximum frequency of PFC switching. Its max frequency limitation is related to the $V_{PFCCOMP}$ and the chart is shown as Fig. 21.

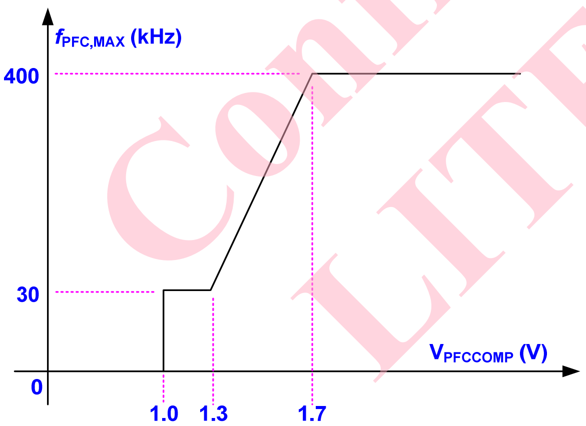


Fig. 21

Flyback Output Voltage Detection and FBAUX OVP

In Power Delivery (PD) application, the output voltage varies from different settings. The chip monitors the output voltage which reflects from secondary to auxiliary winding through the transformer. A voltage detect mechanism is applied on FBAUX pin. The default proportion between V_{OUT} and FBAUX pin is 6.25:1 in typical. While the sampled voltage is higher than $V_{FBAUX,OVP}$ (5.4V) for several cycles, the over voltage protection will be activated. Please refer to Fig. 22, 23 for more detail.

V_{OUT}	V_{FBAUX}
28V	4.48V
20V	3.2V
5V	0.8V

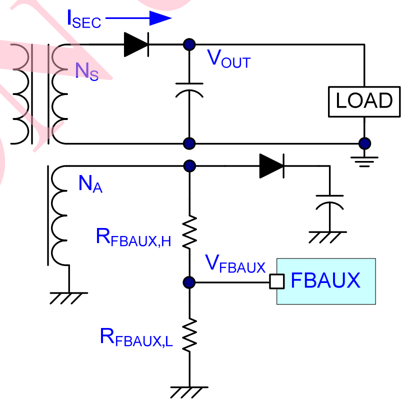


Fig. 22

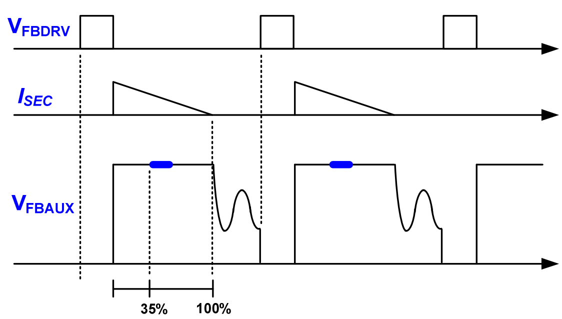


Fig. 23

Flyback Output Current Detection

The IC shows a unique mechanism to measure the real-time output current. Fig. 24, 25 show the schematic and waveform for the operation. By calculating the related parameters, the output current can be obtained as below.

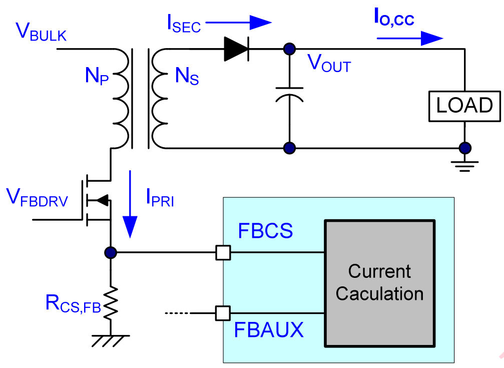


Fig. 24

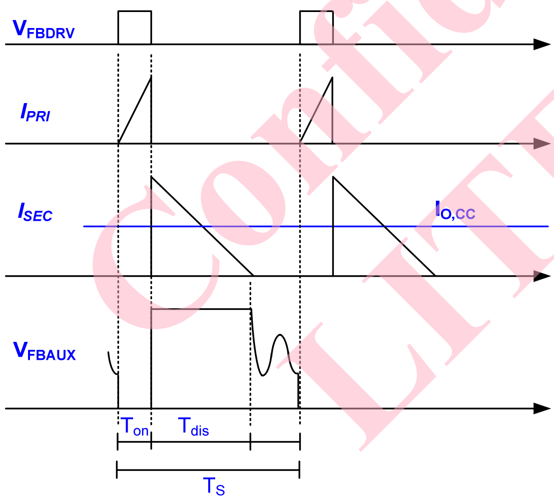


Fig. 25

$$I_{O,CC} \cong \frac{1}{2} \cdot I_{SEC,PK} \cdot \frac{T_{dis}}{T_S} \cong \frac{1}{2} \cdot \left(\frac{N_P}{N_S} \cdot I_{PRI,PK}\right) \cdot \frac{T_{dis}}{T_S}$$

$$\cong \frac{1}{2} \cdot \frac{N_P}{N_S} \cdot \left(\frac{V_{FBCS,PK}}{R_{CS,FB}}\right) \cdot \frac{T_{dis}}{T_S}$$

$$\cong \frac{N_P}{N_S \cdot R_{CS,FB}} \cdot \left(\frac{V_{FBCS,PK}}{2} \cdot \frac{T_{dis}}{T_S}\right)$$

To avoid over current damage, the maximum limit of $\left(\frac{V_{FBCS,PK}}{2} \cdot \frac{T_{dis}}{T_S}\right)$ is 0.22V. By design the N_P, N_S and $R_{CS,FB}$, the max output current can be described as below.

$$I_{O,CC,MAX} \cong \frac{0.22}{R_{CS,FB}} \cdot \frac{N_P}{N_S}$$

H/L line compensation internally on $I_{O,CC,MAX}$ can be preset by different resistance from FBCS pin to ground, which is generally dominant by the low pass filter resistor on FBCS pin. A 450μA current is sourcing out to detect in the first beginning 4ms after brown in. Refer the table as below:

$R_{FBCS-GND}$ (Ω)	$I_{O,CC,MAX}$ Compensation (H/L Line)	
100~220	#1	0% / 0%
330~600	#2	-6% / -4%
820~1200	#3	-14% / -12%

Furthermore, due to the non-idea effects on V_{FBCS} and V_{FBAUX}, the $I_{O,CC,MAX}$ is higher while V_{OUT} is lower. An $I_{O,CC,MAX}$ compensation from H/L V_{OUT} is also obtained. Once the V_{FBAUX} < 1.75V, $I_{O,CC,MAX}$ is internally 20% off to downgrade the protection current level when V_{OUT} is low.

QR Operation with Frequency Limitation

The flyback stage is operating in QR operation to achieve low voltage switching. A frequency limitation depends on V_{FBCOMP} is realized to save the switching loss. In other hand, the frequency limitation varies with V_{FBAUX}, which is related with V_{OUT}. Apply different switching frequency characteristic from different output voltage. The curve chart is shown in Fig. 26. The QR operation characteristic is shown in Fig. 27.

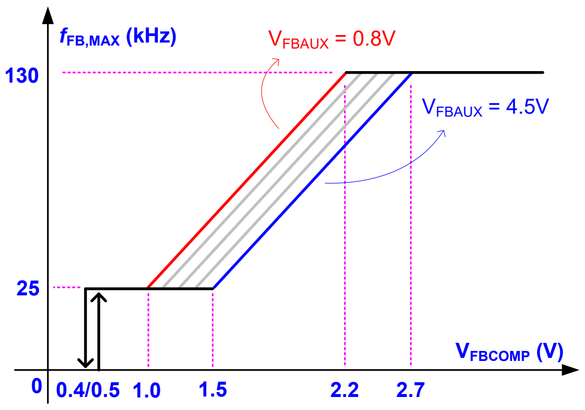


Fig. 26

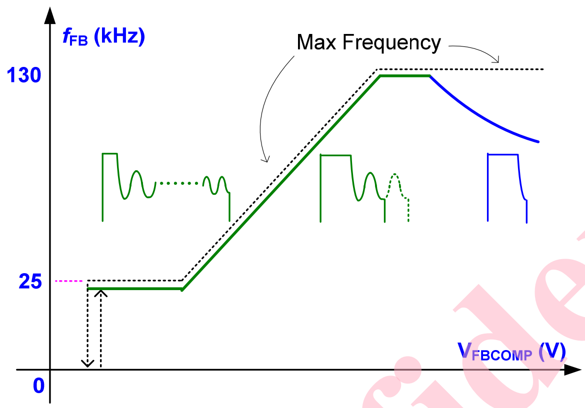


Fig. 27

PFC On/Off Control (SET Pin)

According to output voltage, current and high/low line conditions, the IC features different PFC On/Off settings. The preset chart is chose by different resistors on SET pin. PFC turns on and off characteristic are shown as below.

R_{SET}	PFC On/Off
51kΩ	Fig. 28
68kΩ	Fig. 29
91kΩ	Fig .30
120kΩ	PFC Off *
*: PFC is initially ON while UVLO On	

IC monitors V_{OUT} from FBAUX pin and I_{OUT} from FBAUX, FBCS pin. By a proper design ratio, the internally PFC On/Off setting can be obtained and meets the multi V_{OUT} operation requirements. Furthermore, PFC On/Off can be externally controlled by setting R_{SET}=120kΩ then pulls low SET pin voltage to enable PFC at customized timing.

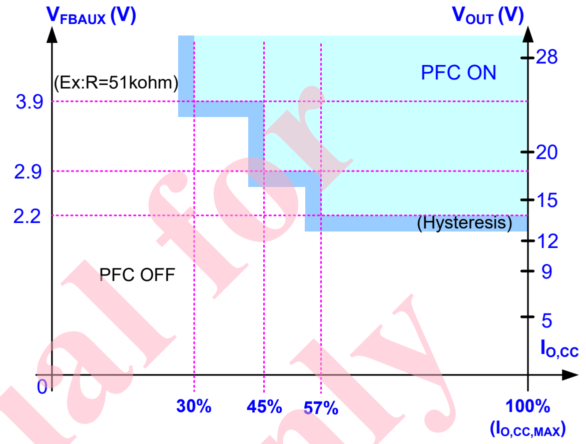


Fig. 28

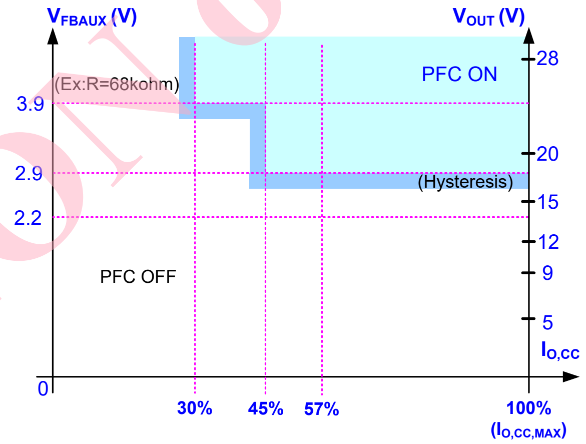


Fig. 29

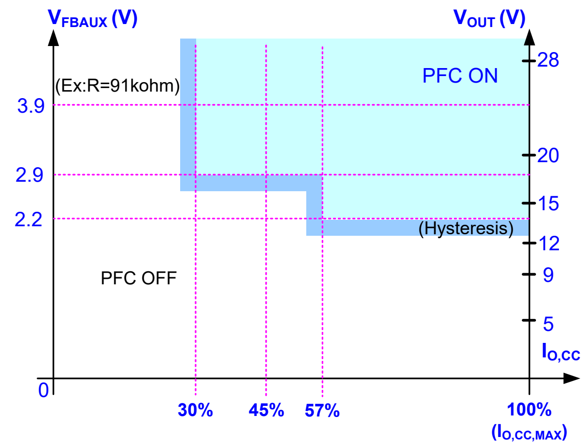


Fig. 30

PFC Off→On De-bounce Time:

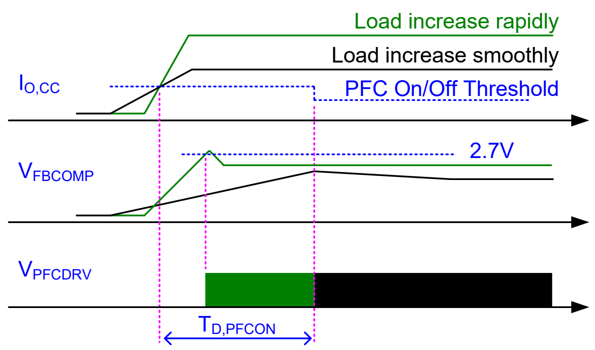


Fig. 31

PFC On→Off De-bounce Time:

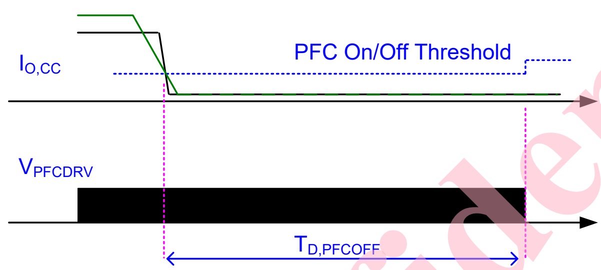


Fig. 32

Once V_{SET} is lower than 0.7V, the PFC starts operating no matter R_{SET} is 51kΩ, 68kΩ, 91kΩ or 120kΩ. While R_{SET}=120kΩ, the PFC is operating in the first 160ms from UVLO On. After that, the PFC is off.

R_{SET} (Ω)	V_{FBAUX} (V)	PFC Off De-bounce Time $T_{D,PFCOFF}$ (sec)
51k 68k 91k	≥ 2.2	10
	< 2.2	0.16
120k	---	0.16

VCC Holding Mode

In Power Delivery (PD) application, the VCC voltage may relative low while V_{OUT} is in lowest stage. A mechanism is obtained to avoid undesirable UVLO Off while doing dynamic load or cable plug in/out. While VCC < 9.5V and V_{FBCOMP} < 0.4V (in burst off), the FBDRV is forced an open-loop switching with 300Hz to maintain the voltage on VCC pin. Once VCC rises to 10.8V or V_{FBCOMP} > 0.5V (out of burst off), the IC resumes to normal close-loop operation.

Internal OTP

An internal OTP (Over Temperature Protection) is built-in, once the temperature of IC chip is higher than 140°C. The auto-recovery protection is triggered, it will stop PFCDRV, FBDRV switching. If the VCC is drop below $V_{CC,OFF}$, the VCC is into hiccup operation and resume switching until the IC temperature is below 140°C. Else if the VCC voltage is kept above $V_{CC,OFF}$, it will recover from internal OTP when the IC temperature is below 100°C.

Flyback Frequency Swapping

The IC is built in a frequency swapping function, which makes it easy for the power supply designers to optimize EMI performance. The frequency swapping is internally set to ±5%.

THDi Optimization

A THDi optimizer is introduced which greatly reduces THDi. Sensing AC sinusoidal signal from HV pin and a related signal is produced to compensate the on-time of PFC stage. When the AC voltage is at its low phase, the PFC turn-on time is increased to compensate the AC input current reduction caused by maximum frequency limit and PFC input capacitor.

X-cap Discharge Current

Connect HV pin to X-cap through diodes and resistors. Once the AC sinusoidal voltage is missing, IC will activate the discharge current to decrease the voltage on X-cap. By this feature, the safety request can be achieve without a bleeding resistor parallel with the X-cap. The no-load power loss can be saved.

AC plug out is triggered on any phase of AC sinusoidal wave. Take 90° for example, Fig. 33, the IC is tracking the sinusoidal status of AC on HV pin. In typical, the HV voltage is rising and falling repeatedly. Once the AC is plug out, the HV voltage is kept on that moment if there is no other discharging path. Without rising & falling voltage on HV pin for over 61ms, the X-cap discharge is activated for 250ms. A sink current on HV pin is enabled.

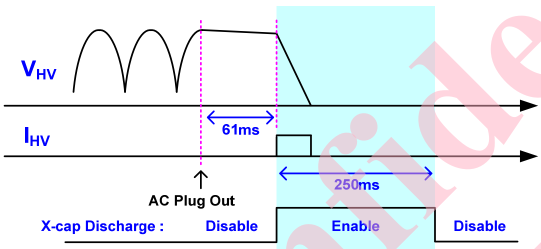


Fig. 33

External Components Selection

The PFCCSZCD pin incorporates the current sense, zero current detection and 2nd PFCOVP in a single pin. Without suitable external components selection, the waveform on this pin may distort and jeopardize its normal operation. To assure a high mass production and temperature consistency, the peripheral capacitors around PFCCSZCD pin, which are $C_{PFCZCD,H}$, $C_{PFCZCD,L}$ and $C_{PFCCSZCD,F}$ in Fig. 20, must be in high precision and low temperature coefficient types. The C0G or its equivalent type is recommended.

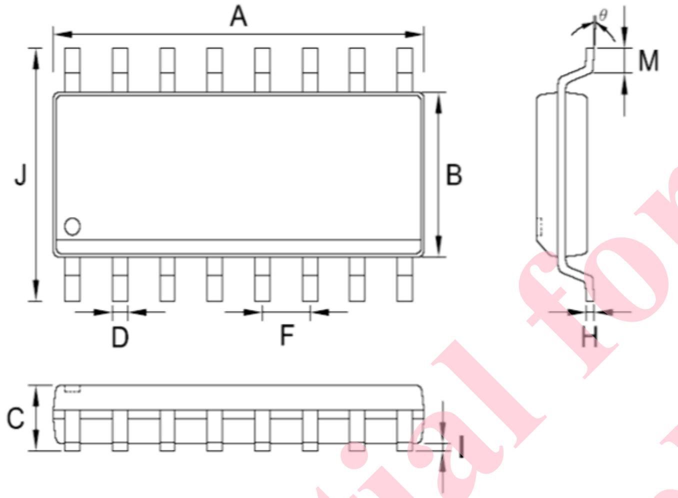
Layout Consideration

The IC has GND and PGND pins to separate the signal ground and power ground. One is for the sensing signal and the other is for MOS driving path.

1. Make the PFCDRV & FBDRV driving loops as small as possible and connect to PGND pin.
2. The MOSFET current paths connect to bulk cap and then back to PGND are recommended.
3. Connect the aux-winding of flyback and VCC/VIN electrolytic capacitors to PGND.
4. A 0.1μF filter capacitor should be placed close to the VCC & GND pin.
5. The MLCC filter capacitors of sensing signals (ex: PFCCSZCD, PFCSNS, FBAUX, FBCOMP & FBCS) connect to GND pin are recommended.
6. Separate GND & PGND loops as two independent groups and connect with a single path.
7. The PFCCSZCD sensing network is extremely vulnerable, so for those high dv/dt traces, such as gate drive, MOSFET drain, should not intertwined with the PFCCSZCD traces and keep separate as possible. Also the PFCCSZCD sensing network shall keep small and short.

Package Information

SOP-16



Symbol	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	9.800	10.010	0.386	0.394
B	3.800	4.000	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.510	0.013	0.020
F	1.27 TYP.		0.05 TYP.	
H	0.178	0.254	0.007	0.010
I	0.100	0.254	0.004	0.010
J	5.790	6.200	0.228	0.244
M	0.380	1.270	0.015	0.050
θ	0°	8°	0°	8°

Revision History

REV.	Date	Change Notice
00	02/03/2023	Original Specification

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Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice.

Customers should verify the datasheets are current and complete before placing order.