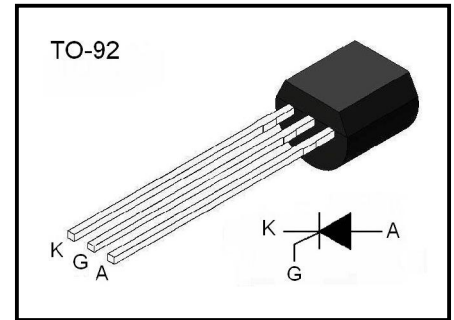


**Description**

The BT169 is glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

**Absolute Maximum Ratings** ( $T_a=25^\circ\text{C}$ )

Parameter	Symbol	Conditions	Value				Unit
			B	D	E	G	
Repetitive peak off-state voltages	$V_{\text{DRM}}, V_{\text{RRM}}$		200	400	500	600	V
Average on-state current	$I_{\text{T(AV)}}$	half sine wave	0.5				A
RMS on-state current	$I_{\text{T(RMS)}}$	all conduction angles	0.8				A
Peak forward surge current	$I_{\text{TSM}}$	$t=10\text{ms}$ , half sine wave	8				A
$I^2t$ for fusing	$I^2t$	$t=10\text{ms}$	0.32				$\text{A}^2\text{s}$
Repetitive rate of rise of on-state current after triggering	$di_{\text{T}}/dt$	$I_{\text{TM}} = 1\text{A}$ , $I_{\text{G}} = 10\text{mA}$ $di_{\text{G}}/dt = 100\text{mA}/\mu\text{s}$	50				$\text{A}/\mu\text{s}$
Peak gate current	$I_{\text{GM}}$		1				A
Peak gate voltage	$V_{\text{GM}}$		5				V
Peak reverse gate voltage	$V_{\text{RGM}}$		5				V
Peak gate power	$P_{\text{GM}}$		2				W
Gate dissipation	$P_{\text{G(AV)}}$	over any 20 ms period	0.1				W
Operating junction temperature	$T_{\text{j}}$		125				$^\circ\text{C}$
Storage temperature range	$T_{\text{stg}}$		-40~+50				$^\circ\text{C}$

**Thermal Characteristics**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Thermal resistance junction-lead	$R_{\theta\text{j-lead}}$				60	$^\circ\text{C}/\text{W}$
Thermal resistance junction-ambient	$R_{\theta\text{j-a}}$	pcb mounted; lead length = 4mm		150		$^\circ\text{C}/\text{W}$

Electrical Characteristics ( $T_j=25^\circ\text{C}$  unless otherwise stated)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Gate trigger current	$I_{GT}$	$V_D=12\text{ V}$ ; $I_T=10\text{ mA}$ ; gate open circuit			200	$\mu\text{A}$
Latching current	$I_L$	$V_D=12\text{ V}$ , $I_{GT}=0.5\text{ mA}$ , $R_{AG} = 1\text{ k}\Omega$			6	$\text{mA}$
Holding current	$I_H$	$V_D=12\text{ V}$ , $I_{GT}=0.5\text{ mA}$ , $R_{AG} = 1\text{ k}\Omega$			5	$\text{mA}$
On state voltage	$V_T$	$I_T=1\text{ A}$			1.35	$\text{V}$
Gate trigger voltage	$V_{GT}$	$V_D=12\text{ V}$ ; $I_T=10\text{ mA}$ ; gate open circuit			0.8	$\text{V}$
Gate non trigger voltage	$V_{GD}$	$V_D=V_{DRM(\text{Max})}$ , $I_T = 10\text{ mA}$ , $T_j = 125^\circ\text{C}$ gate open circuit	0.2			$\text{V}$
Off-state leakage current	$I_D$ , $I_R$	$V_D=V_{DRM(\text{max})}$ , $V_R=V_{RRM(\text{max})}$ $T_j=125^\circ\text{C}$ , $R_{AG} = 1\text{ k}\Omega$			0.1	$\text{mA}$
Critical rate of rise of off-state voltage	$dV_D/dt$	$V_{DM}=67\% V_{DRM(\text{max})}$ ; $T_j = 125^\circ\text{C}$ exponential waveform; $R_{GK}=1\text{ k}\Omega$		25		$\text{V}/\mu\text{s}$
Gate controlled turn-on time	$t_{gt}$	$I_{TM} = 2\text{ A}$ ; $V_D=V_{DRM(\text{max})}$ , $I_G=10\text{ mA}$ $dI_G/dt = 100\text{ mA}/\mu\text{s}$		2		$\mu\text{s}$
Circuit commutated turn-off time	$t_q$	$V_{DM}=67\% V_{DRM(\text{max})}$ ; $T_j = 125^\circ\text{C}$ $I_{TM} = 2\text{ A}$ ; $V_R = 35\text{ V}$ ; $dI_{TM}/dt = 30\text{ A}/\mu\text{s}$ $dV_D/dt=2\text{ V}/\mu\text{s}$ ; $R_{GK}=1\text{ k}\Omega$		100		$\mu\text{s}$

Typical Characteristics

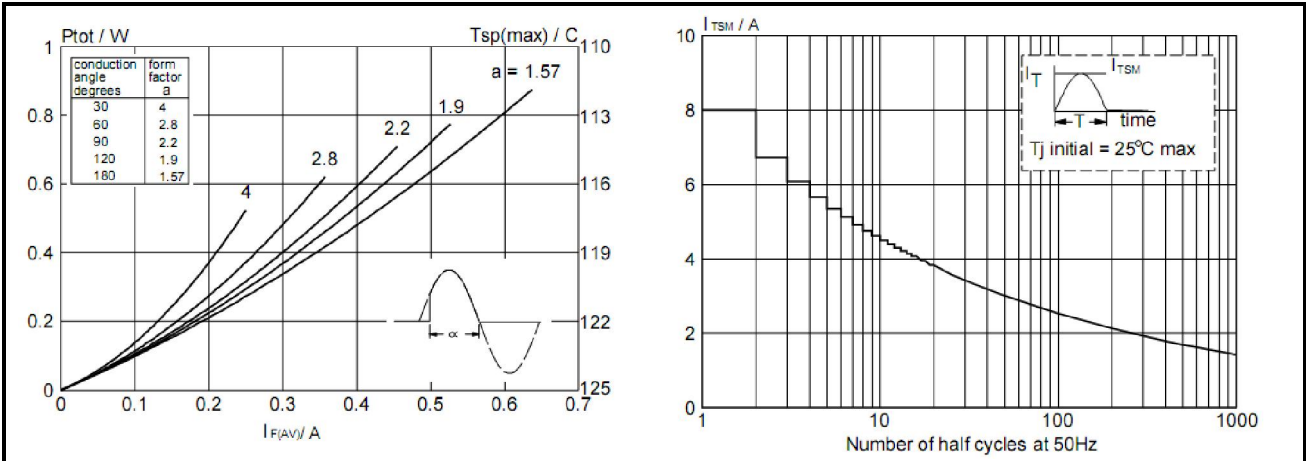


Fig.1. Maximum on-state dissipation,  $P_{tot}$ , vs average on-state current,  $I_{T(AV)}$ , where  $a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$ .

Fig.2. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , vs. number of cycles, for sinusoidal currents,  $f = 50$  Hz.

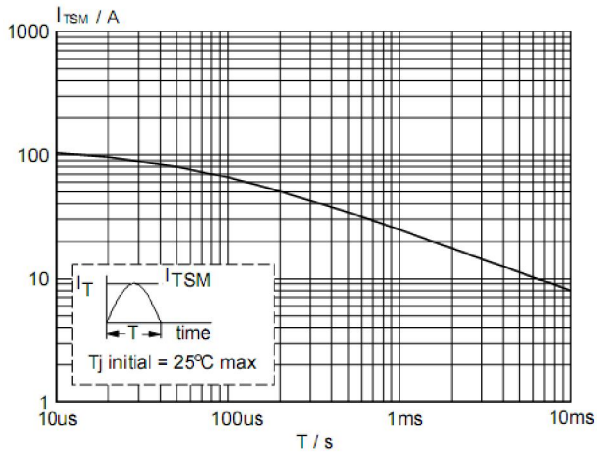


Fig.3. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , vs pulse width  $t_p$ , for sinusoidal currents,  $t_p \leq 10$ ms.

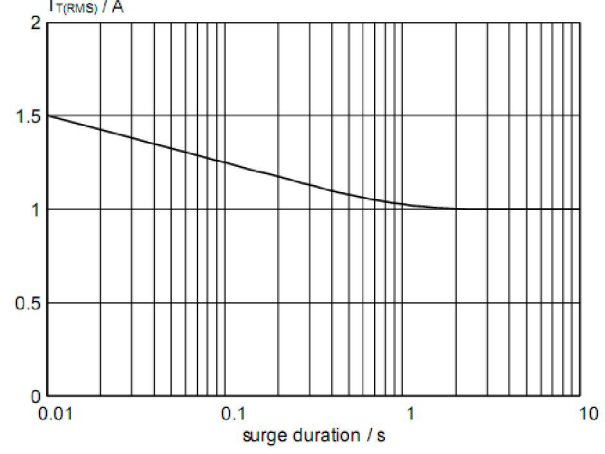


Fig.4. Maximum permissible repetitive rms on-state current  $I_{T(RMS)}$ , vs surge duration, for sinusoidal currents,  $f = 50$  Hz;  $T_{sp} \leq 112^\circ\text{C}$ .

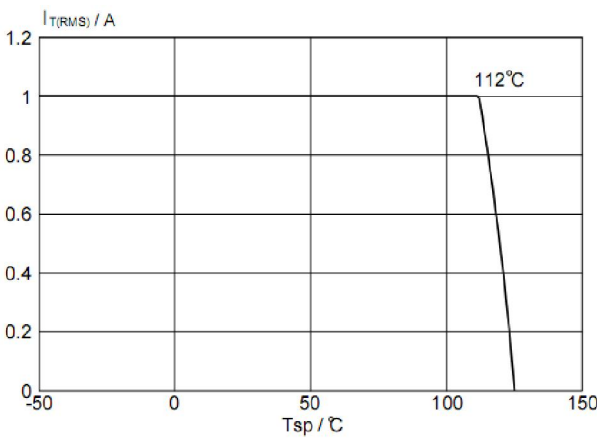


Fig.5. Maximum permissible rms current  $I_{T(RMS)}$ , vs solder point temperature  $T_{sp}$ .

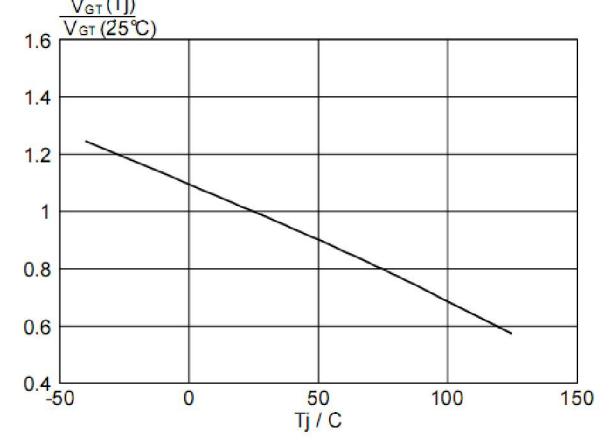


Fig.6. Normalised gate trigger voltage  $V_{GT}(T_j) / V_{GT}(25^\circ\text{C})$ , vs junction temperature  $T_j$ .

Typical Characteristics

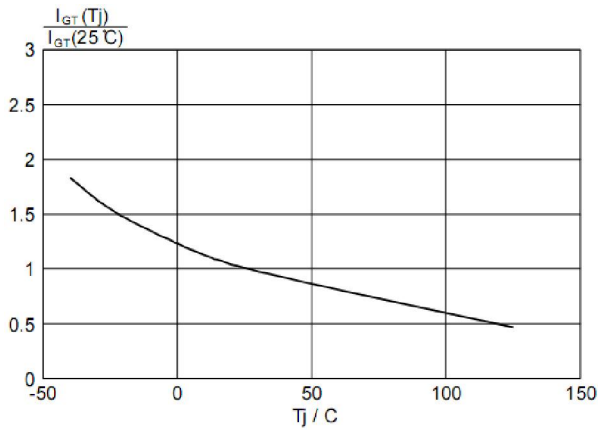


Fig.7. Normalised gate trigger current  $I_{GT}(T_j) / I_{GT}(25^\circ\text{C})$ , vs junction temperature  $T_j$ .

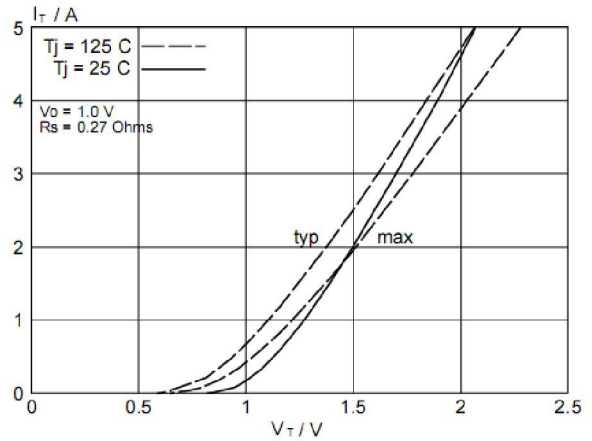


Fig.8. Typical and maximum on-state characteristic.

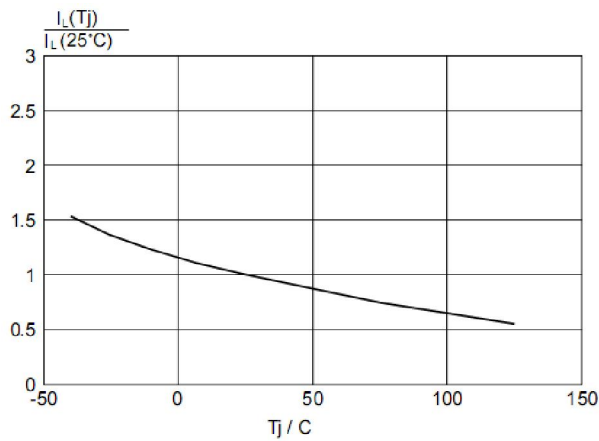


Fig.9. Normalised latching current  $I_L(T_j) / I_L(25^\circ\text{C})$ , vs  $T_j$ ,  $R_{GK} = 1 \text{ k}\Omega$ .

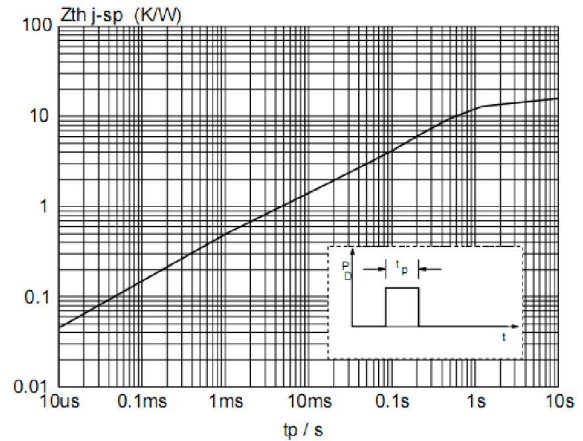


Fig.10. Transient thermal impedance  $Z_{th\ j-sp}$ , vs pulse width  $t_p$ .

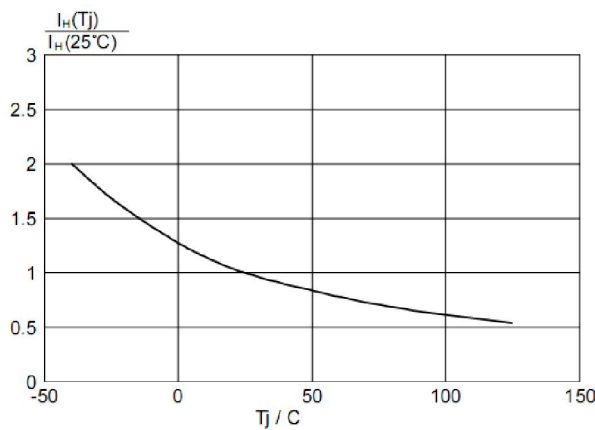


Fig.11. Normalised holding current  $I_H(T_j) / I_H(25^\circ\text{C})$ , vs  $T_j$ ,  $R_{GK} = 1 \text{ k}\Omega$ .

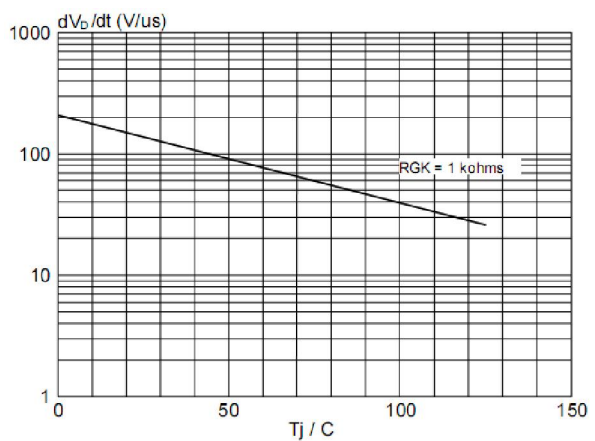
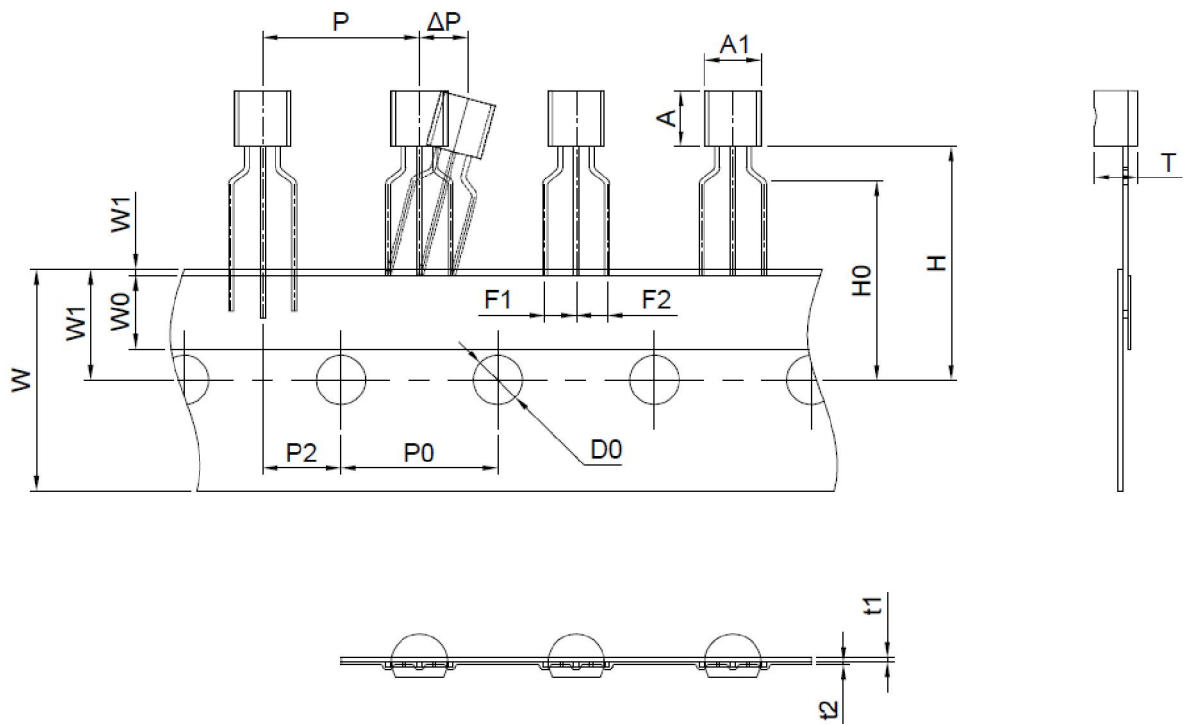


Fig.12. Typical, critical rate of rise of off-state voltage,  $dV_D/dt$  vs  $T_j$

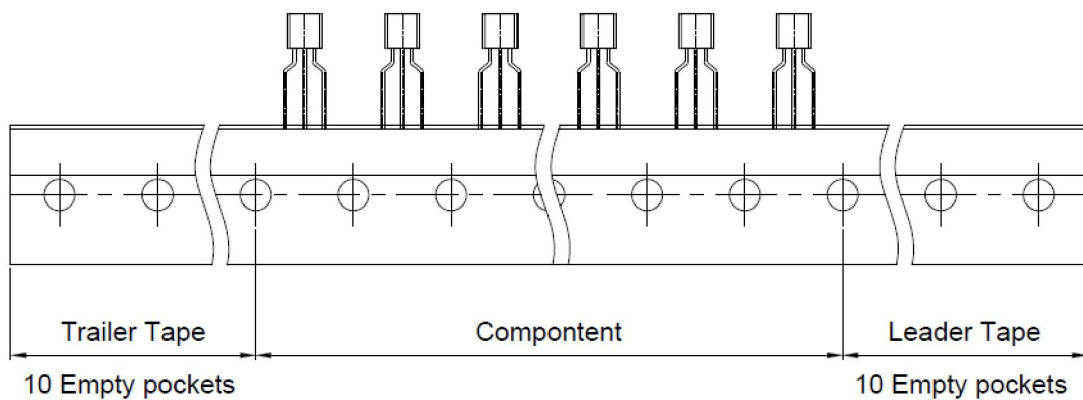
**Package Dimensions**

Dim	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	3.30	3.70	0.130	0.146
A1	2.30	2.70	0.091	0.106
b	0.40	0.50	0.016	0.020
b1	0.50	0.70	0.020	0.028
c	0.35	0.45	0.014	0.018
D	4.45	4.70	0.175	0.185
E	4.40	4.65	0.173	0.183
e	1.17	1.37	0.046	0.054
e1	2.34	2.64	0.092	0.104
L	13.50	14.50	0.531	0.571
L1	1.80	2.20	0.071	0.087

Taping Dimensions



Dimensions are in millimeter								
A	A1	T	P	P0	P2	F1	F2	W
4.6	4.6	3.5	12.7	12.7	6.35	2.54	2.54	18.0
W0	W1	W2	H	H0	D0	t1	T2	ΔP
6.0	9.0	1.0Max	19.0	18.0	4.0	0.4	0.2	0



Package	Box	Box Size(mm)	Carton	Carton Size(mm)
TO-92	2000pcs	330×145×45	20,000pcs	360×330×240