

FDWS9509L-F085-VB Datasheet

P-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A)	Q _g (Typ.)
- 40	0.010 at V _{GS} = - 10 V	- 40	42.6 nC
	0.012 at V _{GS} = - 4.5 V	- 35	

FEATURES

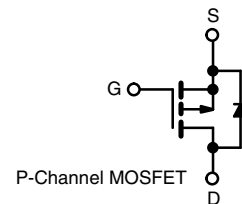
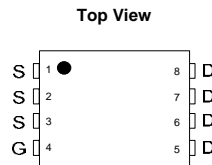
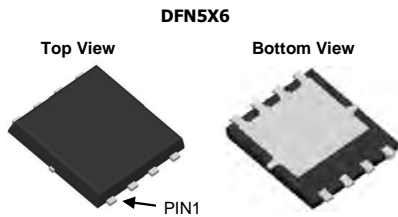
- Halogen-free According to IEC 61249-2-21 Definition
- Trench Power MOSFET
- 100% R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load Switch
- Motor Drives



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	- 40	V
Gate-Source Voltage		V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	- 40	A
	T _C = 70 °C		- 32	
	T _A = 25 °C		- 14.6 ^{a, b}	
	T _A = 70 °C		- 11.3 ^{a, b}	
Pulsed Drain Current (t = 300 μs)		I _{DM}	- 70	A
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	- 35 ^d	
	T _A = 25 °C		- 4.3 ^{a, b}	
Avalanche Current		I _{AS}	- 30	mJ
Single-Pulse Avalanche Energy		E _{AS}	45	
Maximum Power Dissipation	T _C = 25 °C	P _D	39	W
	T _C = 70 °C		25	
	T _A = 25 °C		5 ^{a, b}	
	T _A = 70 °C		3.2 ^{a, b}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{e, f}			260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, c}		R _{thJA}	20	25	°C/W
Maximum Junction-to-Case					

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- The DFN5x6 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 54 °C/W.

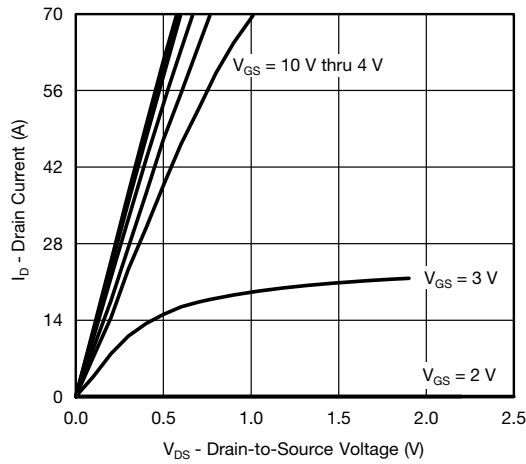
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0, I_D = -250\text{ }\mu\text{A}$	-40			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-33		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		5			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1.2		-2.3	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq -10\text{ V}, V_{GS} = -10\text{ V}$	-30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -15\text{ A}$		0.010		Ω
		$V_{GS} = -4.5\text{ V}, I_D = -10\text{ A}$		0.012		
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -15\text{ A}$		40		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		3650		pF
Output Capacitance	C_{oss}			386		
Reverse Transfer Capacitance	C_{rss}			350		
Total Gate Charge	Q_g	$V_{DS} = -20\text{ V}, V_{GS} = -10\text{ V}, I_D = -10\text{ A}$		86	134	nC
				42.6	63	
Gate-Source Charge	Q_{gs}	$V_{DS} = -20\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -10\text{ A}$		10		
Gate-Drain Charge	Q_{gd}			19.8		
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.4	1.5	3.0	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		15	30	ns
Rise Time	t_r			14	28	
Turn-Off Delay Time	$t_{d(off)}$			56	110	
Fall Time	t_f			11	22	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		60	110	
Rise Time	t_r			56	110	
Turn-Off Delay Time	$t_{d(off)}$			50	100	
Fall Time	t_f			22	40	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			-50	A
Pulse Diode Forward Current	I_{SM}				-70	
Body Diode Voltage	V_{SD}	$I_S = -3\text{ A}, V_{GS} = 0$		-0.74	-1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		29	55	ns
Body Diode Reverse Recovery Charge	Q_{rr}			25	46	nC
Reverse Recovery Fall Time	t_a			16		ns
Reverse Recovery Rise Time	t_b			13		

Notes:

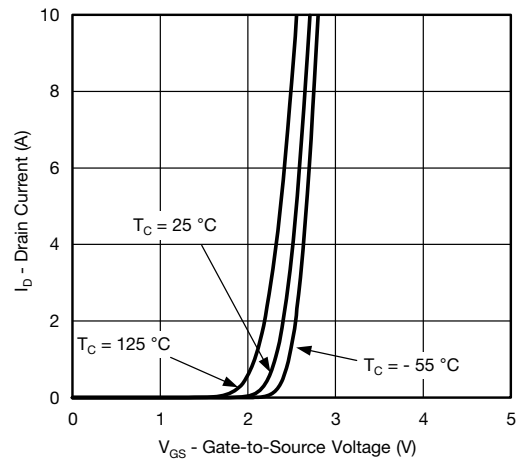
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

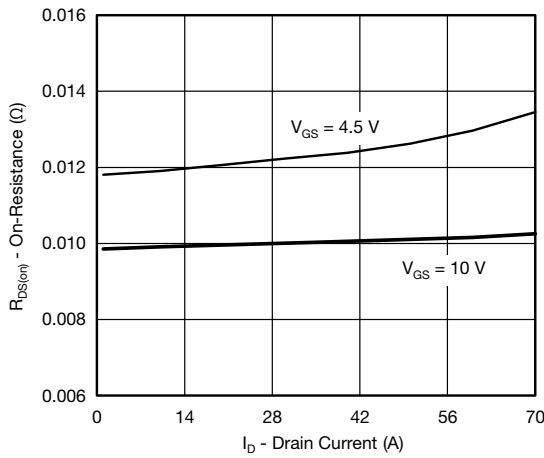
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



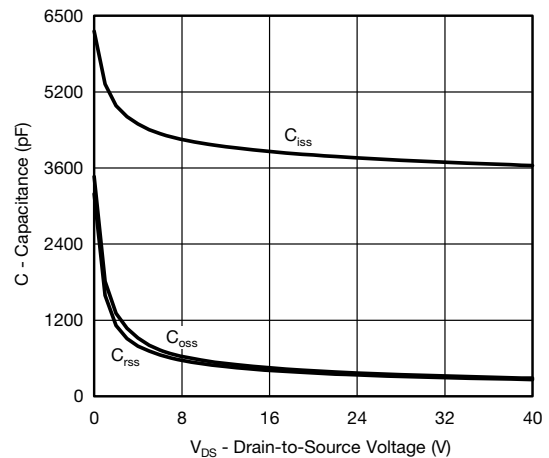
Output Characteristics



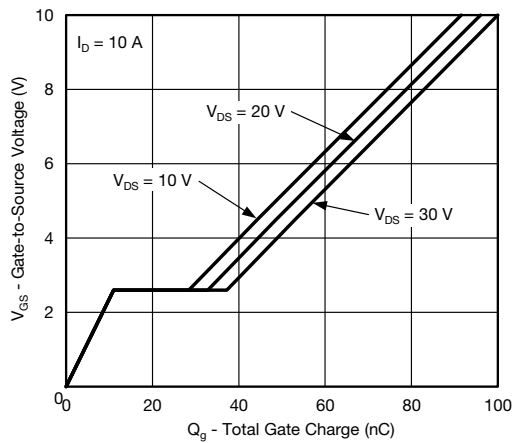
Transfer Characteristics



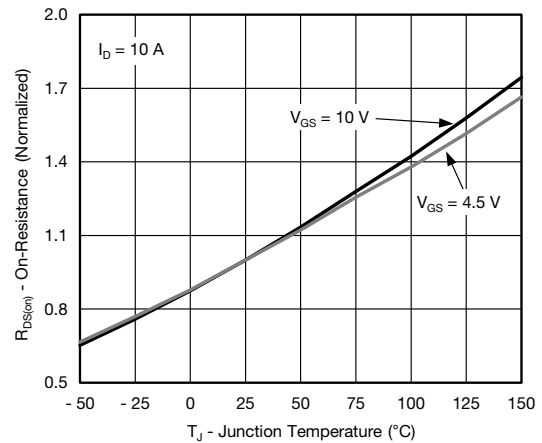
On-Resistance vs. Drain Current



Capacitance

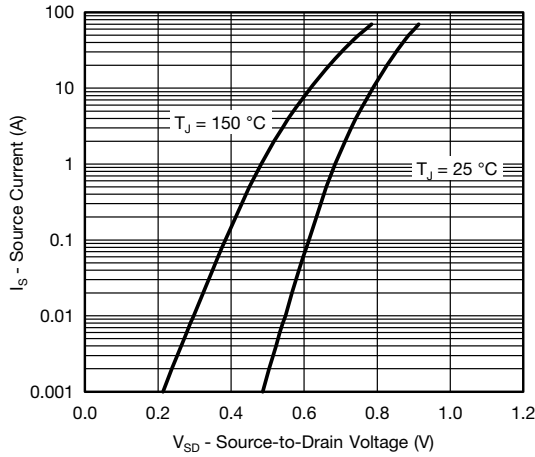


Gate Charge

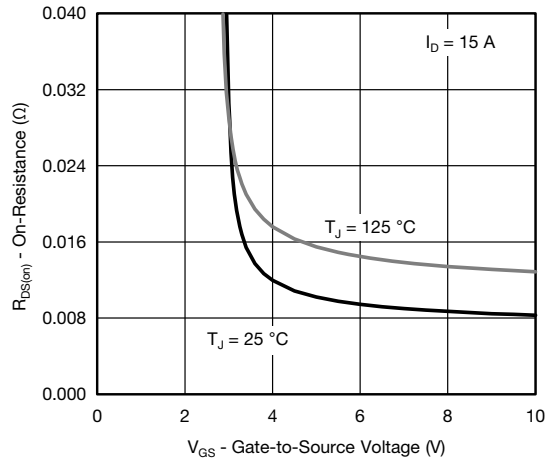


On-Resistance vs. Junction Temperature

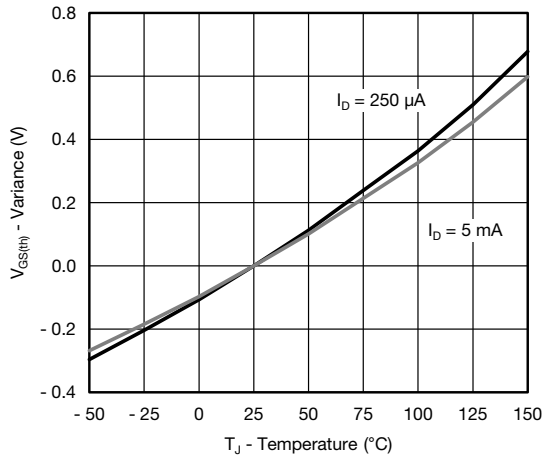
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



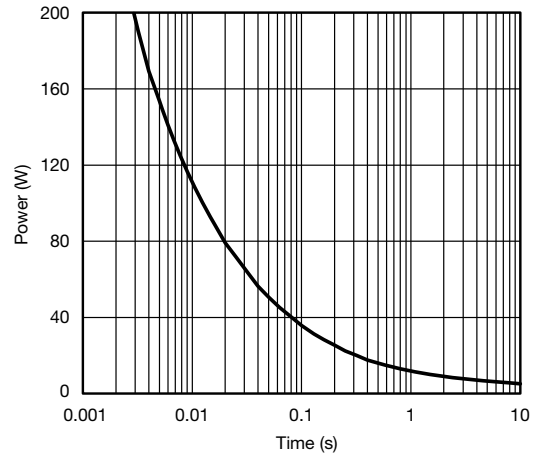
Source-Drain Diode Forward Voltage



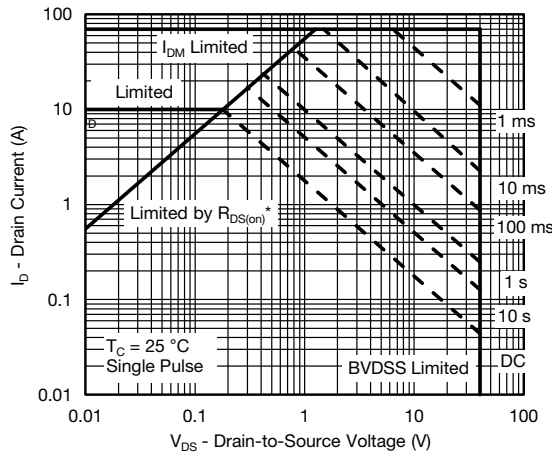
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



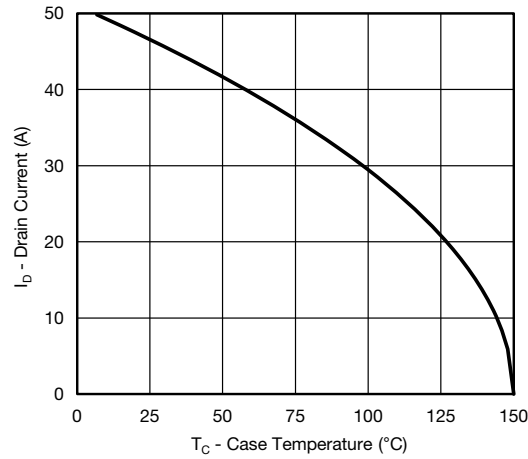
Single Pulse Power, Junction-to-Ambient



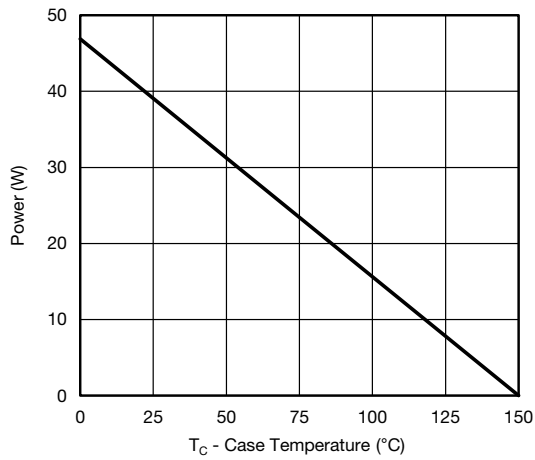
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

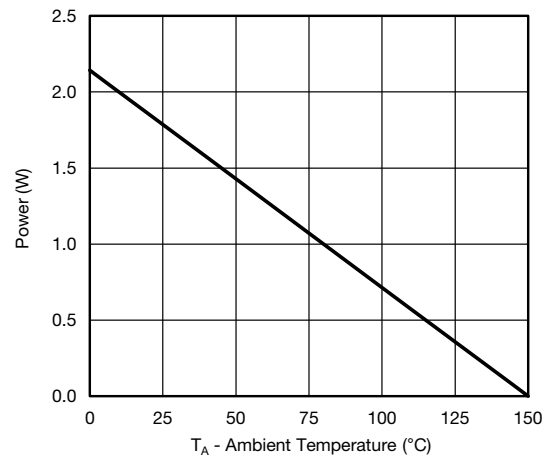
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



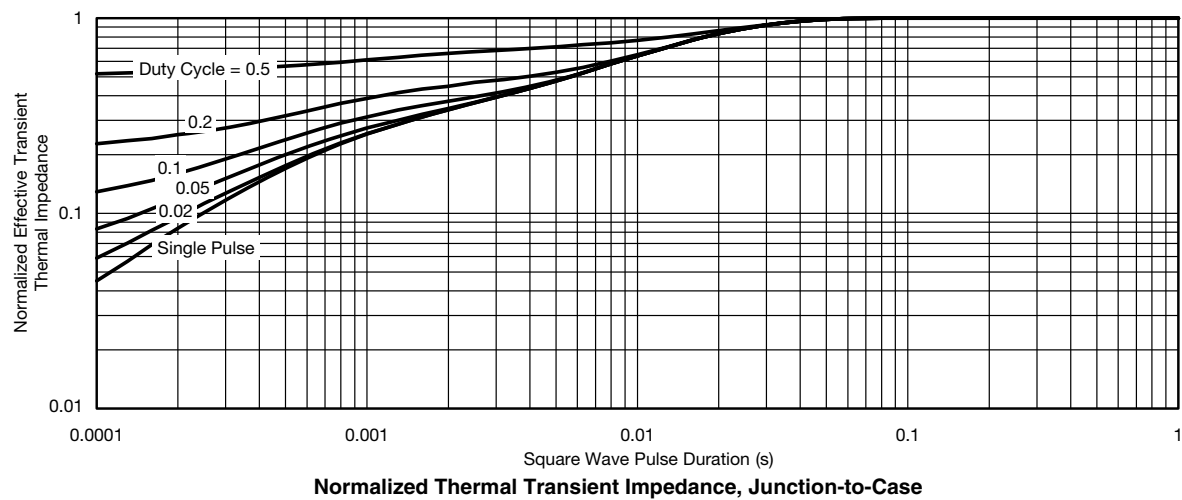
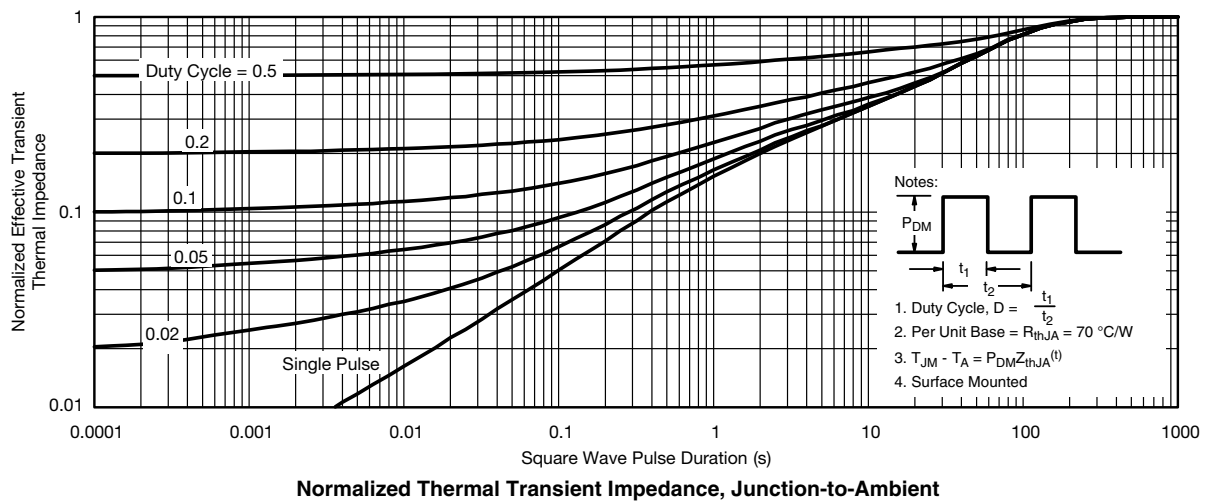
Power, Junction-to-Case



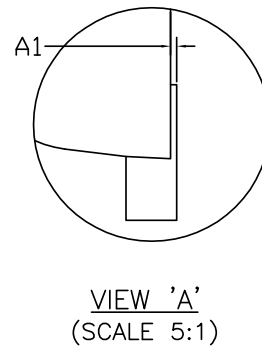
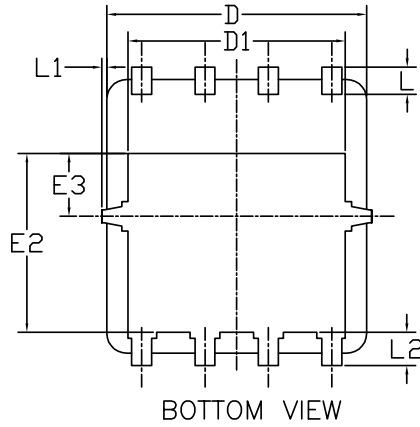
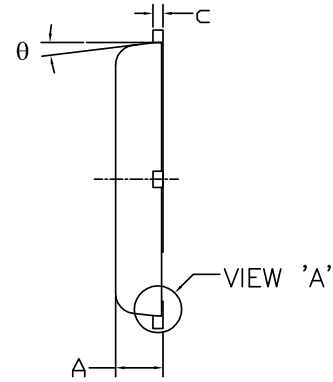
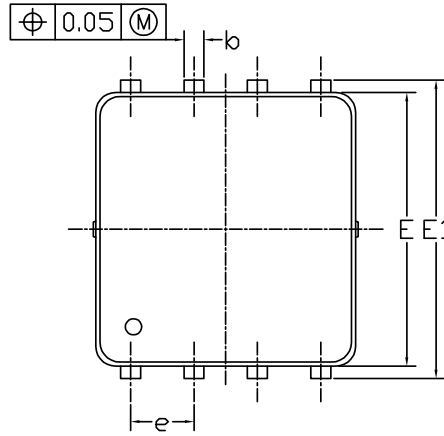
Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on T_{J(max)} = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

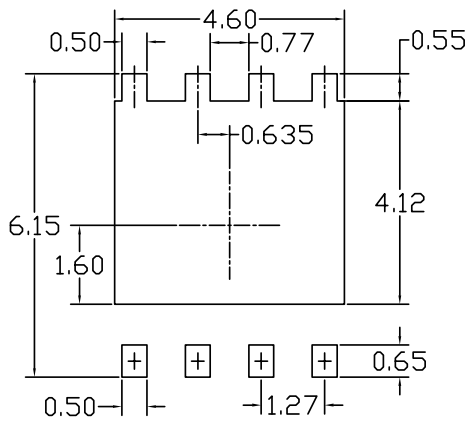
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



DFN5x6_8L_EP1_P PACKAGE OUTLIN



RECOMMENDED LAND PATTERN



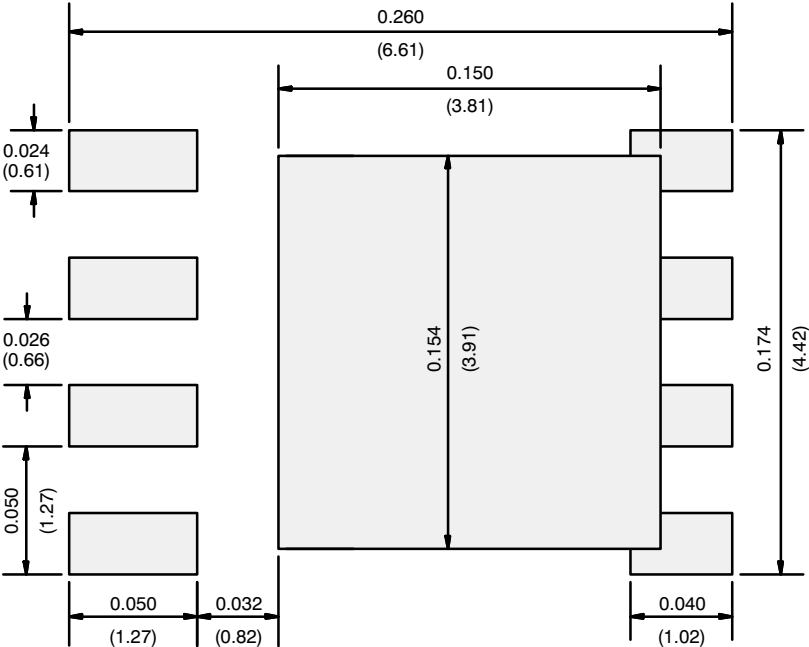
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.95	1.00	0.033	0.037	0.039
A1	0.00	---	0.05	0.000	---	0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.10	5.20	5.30	0.201	0.205	0.209
D1	4.25	4.35	4.45	0.167	0.171	0.175
E	5.45	5.55	5.65	0.215	0.219	0.222
E1	5.95	6.05	6.15	0.234	0.238	0.242
E2	3.525	3.625	3.725	0.139	0.143	0.147
E3	1.175	1.275	1.375	0.046	0.050	0.054
e	1.27 BSC			0.050 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0	---	0.15	0	---	0.006
L2	0.68 REF			0.027 REF		
θ	0°	---	10°	0°	---	10°

UNIT: mm

NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
2. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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