RORKE Memory Module Datasheet

RDRMD5064G5600RA
DDR5-5600（CL46）288-pin RDIMM
64GB
(4096M x 80-bit)

Version:V1.0

Version	Changes	Page	Date
V1.0	1st release	-	2026/3/4

Table of Contents

1. General Description

RDRMD5064G5600RA is DDR5-5600(CL46)-45-45 SDRAM memory module. The SPD is programmed to JEDEC standard latency 5600Mbps timing of 46-45-45 at 1.1V. The module is composed of 20pcs 32Gb CMOS DDR5 SDRAMs in FBGA package, one JEDEC compliant DDR5 register driver and one 8Kbit EEPROM in 8pin TDFN package on a 288pin glass–epoxy printed circuit board.

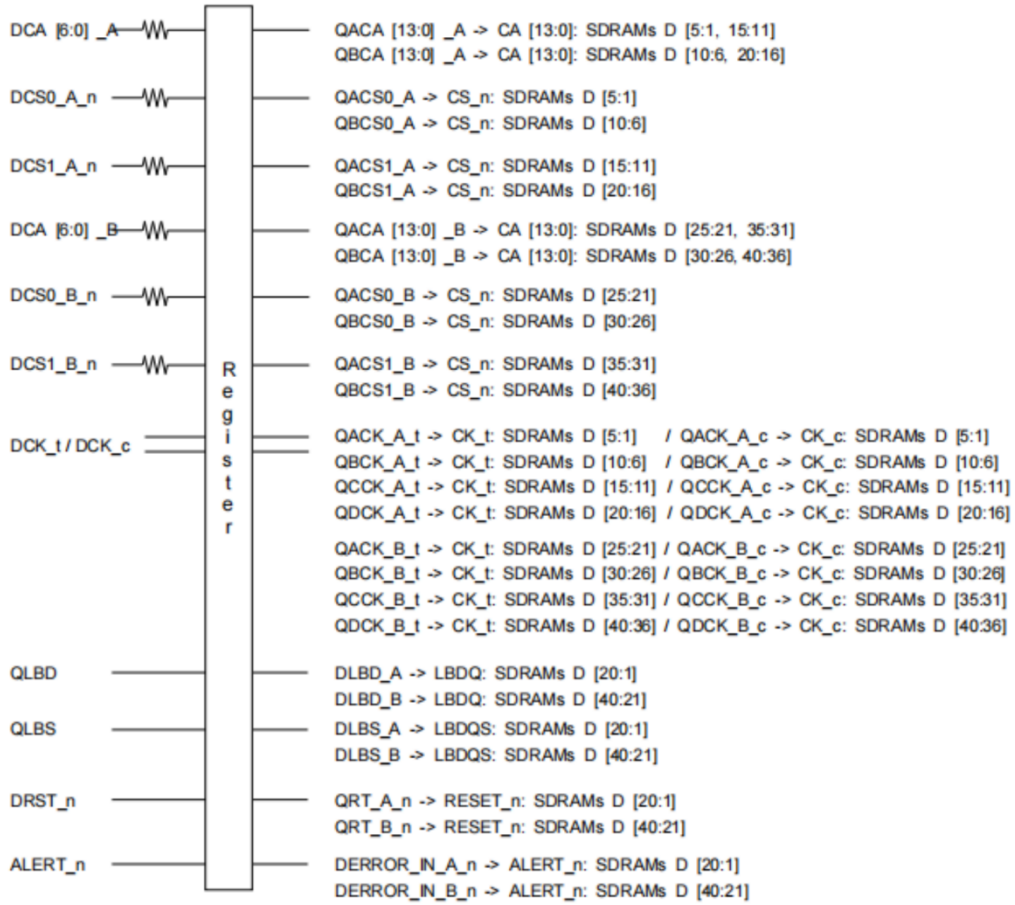
The module is a Dual In-line Memory Module and intended for mounting onto 288 pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

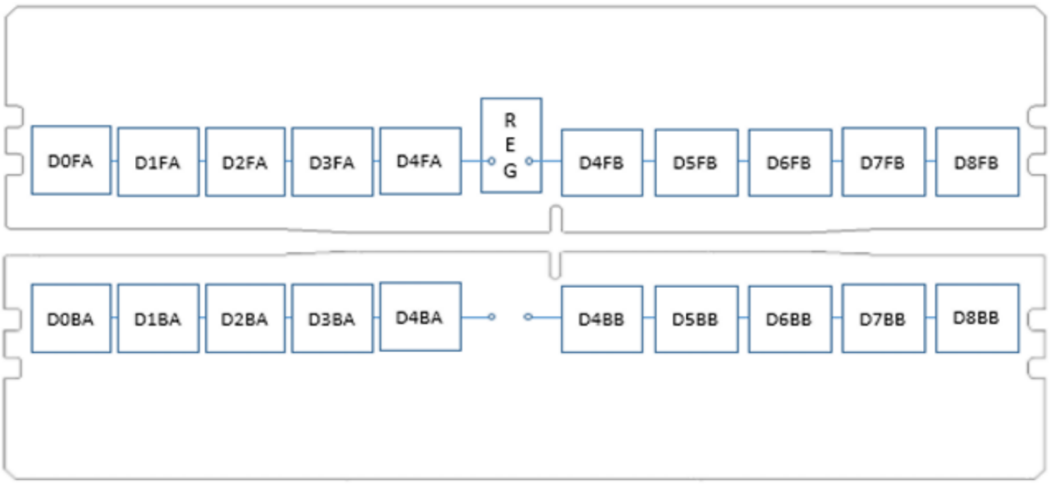
2. Features

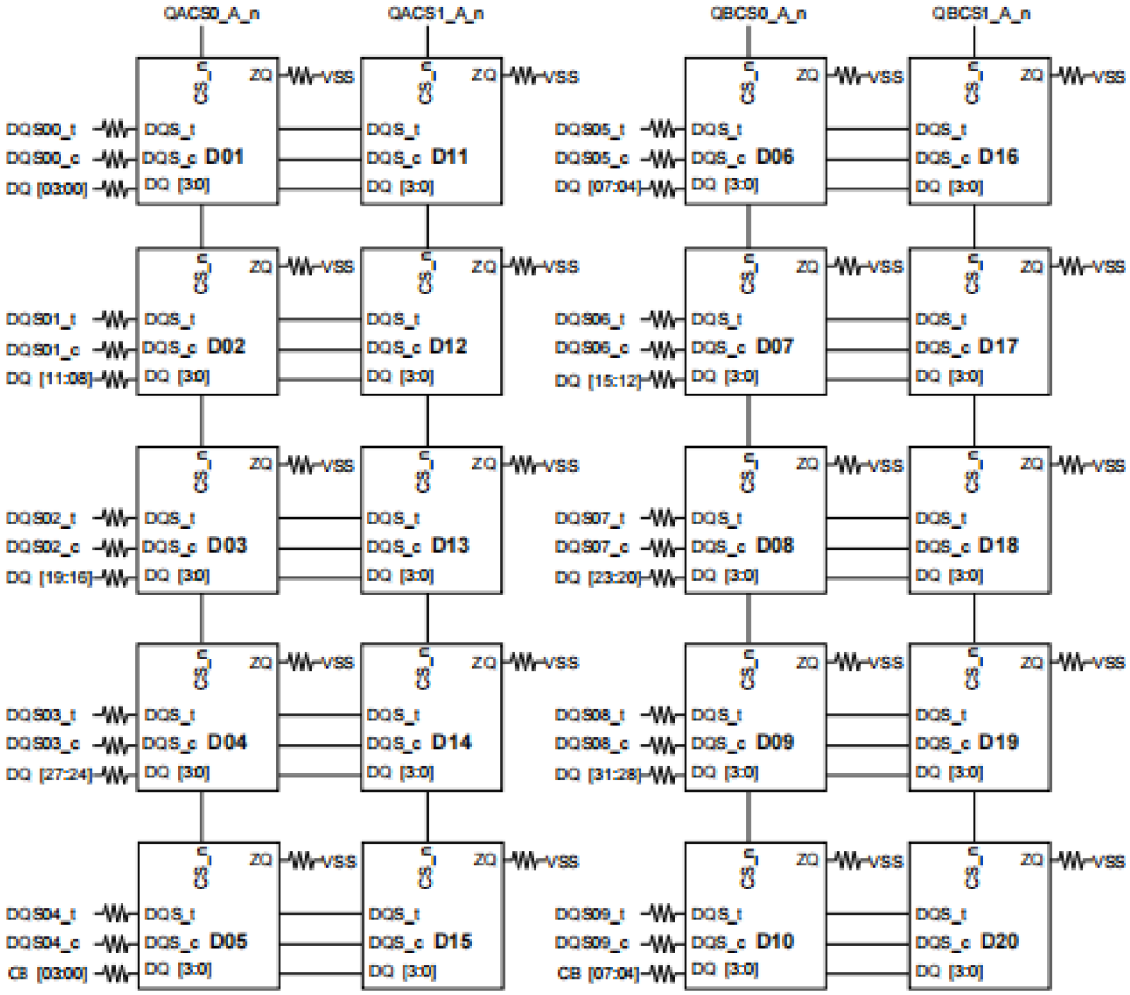
- DRAM VDD/VDDQ = 1.1V (-33mV / +67mV)
- DRAM VPP = 1.8V (–54mV / +108mV)
- 32 Bank with x4/x8
- 16 Bank with x16
- 8 BG(Bank Group) for X4/X8/X16 configurations
- BL16, BC8 OTF, BL32, BL32 OTF supported
- Temperature Encoding
- Same Bank Refresh
- VrefDQ / VrefCA / VrefCS Training
- Hard/Soft Post Package Repair
- Input Clock Frequency Change
- Maximum Power Saving Mode (MPSM)
- Multi-Purpose Command (MPC)
- Per DRAM Addressability (PDA)
- Read Training Mode
- CA Training Mode
- CS Training Mode
- Per Pin VREFDQ Training
- Write Leveling Training Mode
- Connectivity Test (CT)
- ZQ Calibration
- DFE (Decision Feedback Equalization) for DQ

- DQS Interval Oscillator
- 1N / 2N Mode support for Commands
- On-Die ECC
- ECC Transparency and Error Scrub
- CRC (Cyclic Redundancy Check)
- Loopback for multiple purposes - monitor data, BER(Bit Error Rate) analysis, etc.
- Package Output Driver Test Mode
- Training Modes:
  - VrefDQ / VrefCA / VrefCS Training
  - Read Training Mode
  - CA Training Mode
  - CS Training Mode
  - Per Pin VREFDQ Training
  - Write Leveling Training Mode
  - Duty Cycle Adjuster (DCA) for Read - Global
  - Per Pin DCA(Duty Cycle Adjuster) for Read - Per Pin(DQ)
- NOT required RFM

3. Block Diagram







Note 1: Unless otherwise noted resistors are 15 Ω ± 5%

Note 2: ZQ resistors are 240 Ω ± 1%.

4. Pin Assignments

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
1	VIN_BULK	145	VIN_BULK	74	PAR_A	218	CK_c
2	RFU	146	VIN_BULK	75	VSS	219	VSS
3	VIN_MGMT	147	PCAMP	KEY			
4	HSCL	148	HSA				
5	HSDA	149	RFU	76	CA0_B	220	RFU
6	VSS	150	RFU	77	VSS	221	CA1_B
7	DQ1_A	151	VSS	78	CA2_B	222	VSS
8	VSS	152	DQ2_A	79	VSS	223	CA3_B
9	DQ1_A	153	VSS	80	CA4_B	224	VSS
10	VSS	154	DQ3_A	81	VSS	225	CA5_B
11	DQS0_A_T	155	VSS	82	CA6_B	226	VSS
12	DQS0_A_c	156	DQS5_A_c, TDQS5_A_c	83	VSS	227	PAR_B
13	VSS	157	DQS5_A_T, TDQS5_A_T	84	CS0_B_n	228	VSS
14	DQ4_A	158	VSS	85	VSS	229	CS1_B_n
15	VSS	159	DQ6_A	86	DLBDQ	230	VSS
16	DQ5_A	160	VSS	87	DLBDQS	231	RFU
17	VSS	161	DQ7_A	88	VSS	232	RFU
18	DQ8_A	162	VSS	89	CB4_B	233	VSS
19	VSS	163	DQ10_A	90	VSS	234	CB6_B
20	DQ9_A	164	VSS	91	CB5_B	235	VSS
21	VSS	165	DQ11_A	92	VSS	236	CB7_B
22	DQS1_A_t	166	VSS	93	DQS9__B_t, TDQS9__B_t	237	VSS
23	DQS1_A_C	167	DQS6_A_c, TDQS6_A_c	94	DQS9_B_C, TDQS9_B_C	238	DQS4__B_c
24	VSS	168	DQS6_A_t, TDQS6_A_t	95	VSS	239	DQS4__B_t
25	DQ12_A	169	VSS	96	CB0_B	240	VSS
26	VSS	170	DQ14_A	97	VSS	241	CB2_B
27	DQ13_A	171	VSS	98	CB1_B	242	VSS
28	VSS	172	DQ15_A	99	VSS	243	CB3_B
29	DQ16_A	173	VSS	100	DQ0_B	244	VSS
30	VSS	174	DQ18_A	101	VSS	245	DQ2_B
31	DQ17_A	175	VSS	102	DQ1_B	246	VSS
32	VSS	176	DQ19_A	103	VSS	247	DQ3_B
33	DQS2_A_t	177	VSS	104	DQS0__B_t	248	VSS
34	DQS2_A_c	178	DQS7_A_C, TDQS7_A_C	105	DQS0__B_c	249	DQS5_B_c, TDQS5_B_c

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
35	VSS	179	DQS7_A_t, TDQS7_A_t	106	VSS	250	DQS5_B_t, TDQS5_B_t
36	DQ20_A	180	VSS	107	DQ4_B	251	VSS
37	VSS	181	DQ22_A	108	VSS	252	DQ6_B
38	DQ21_A	182	VSS	109	DQ5_B	253	VSS
39	VSS	183	DQ23_A	110	VSS	254	DQ7_B
40	DQ24_A	184	VSS	111	DQ8_B	255	VSS
41	VSS	185	DQ26_A	112	VSS	256	DQ10_B
42	DQ25_A	186	VSS	113	DQ9_B	257	VSS
43	VSS	187	DQ27_A	114	VSS	258	DQ11_B
44	DQS3_A_T	188	VSS	115	DQS1_B_T	259	VSS
45	DQS3_A_c	189	DQS8_A_c, TDQS8_A_c	116	DQS1_B_c	260	DQS6_B_c, TDQS6_B_c
46	VSS	190	DQS8_A_T, TDQS8_A_T	117	VSS	261	DQS6_B_T, TDQS6_B_T
47	DQ28_A	191	VSS	118	DQ12_B	262	VSS
48	VSS	192	DQ30_A	119	VSS	263	DQ14_B
49	DQ29_A	193	VSS	120	DQ13_B	264	VSS
50	VSS	194	DQ31_A	121	VSS	265	DQ15_B
51	CB0_A	195	VSS	122	DQ16_B	266	VSS
52	VSS	196	CB2_A	123	VSS	267	DQ18_B
53	CB1_A	197	VSS	124	DQ17_B	268	VSS
54	VSS	198	CB3_A	125	VSS	269	DQ19_B
55	DQS4_A_t	199	VSS	126	DQS2_B_t	270	VSS
56	DQS4_A_c	200	DQS9_A_c, TDQS9_A_c	127	DQS2_B_C	271	DQS7_B_c, TDQS7_B_c
57	VSS	201	DQS9_A_t, TDQS9_A_t	128	VSS	272	DQS7_B_t, TDQS7_B_t
58	CB4_A	202	VSS	129	DQ20_B	273	VSS
59	VSS	203	CB6_A	130	VSS	274	DQ22_B
60	CB5_A	204	VSS	131	DQ21_B	275	VSS
61	VSS	205	CB7_A	132	VSS	276	DQ23_B
62	ALERT_n	206	VSS	133	DQ24_B	277	VSS
63	VSS	207	RESET_n	134	VSS	278	DQ26_B
64	CS0_A_n	208	VSS	135	DQ25_B	279	VSS
65	VSS	209	CS1_A_n	136	VSS	280	DQ27_B
66	CA0_A	210	VSS	137	DQS3_B_t	281	VSS
67	VSS	211	CA1_A	138	DQS3_B_c	282	DQS8_B_c, TDQS8_B_c
68	CA2_A	212	VSS	139	VSS	283	DQS8_B_t, TDQS8_B_t
69	VSS	213	CA3_A	140	DQ28_B	284	VSS

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
70	CA4_A	214	VSS	141	VSS	285	DQ30_B
71	VSS	215	CA5_A	142	DQ29_B	286	VSS
72	CA6_A	216	VSS	143	VSS	287	DQ31_B
73	VSS	217	CK_t	144	RFU	288	VSS

5. Pin Description

Pin Name	Function
CK_t, CK_c,	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA[6:0] A CA[6:0]_B	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle,the pins may not be interchanged between devices on the same bus. The address inputs also provide the opcode during Mode Register Set commands.
CS[1:0] A CS[1:0]_B	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command codes. CS_n is also used to enter and exit the parts from power down mode and self-refresh mode. While not in self-refresh mode the CS_n input buffer operates with the same ODT and VREF parameters as configured by the CA_ODT strap setting or mode register. When in self-refresh the CS_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
PAR A PAR_B	Command and Address Parity Input: DDR5 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CSx__x__n LOW
ALERT_n	Alert: If there is an error in CRC, then ALERT_n shall drive LOW for the period time interval and return HIGH. During Connectivity Test mode, this pin functions as an input. Usage of this signal or not is system dependent. In case this pin is not connected, ALERT_n pin must be bonded to VDDQ on the system board.
RESET_n	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ.
PCAMP	Control and Monitor Port. Provides three different functions: (1) Register write protect function; (2) Fail_n function; and (3) Status function (PWR_GOOD).
HSCL	Bus clock used to strobe data into HUB device. When open drain, a pullup resistor is required on the system motherboard.
HSDA	I2C/I3C-Basic data. When Open drain, a pullup resistor is required on the system motherboard.
HSA	Device address for the HUB. Tied to GND through resistor for HID in normal operation and directly to

	GND in tester operation
DQ[31:0]_A DQ[31:0]_B	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register, then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
CB[7:0]_A CB[7:0]_B	ECC Checkbits Input/ Output: Bi-directional data bus - for 8-bit ECC (EC8) all 8 bits are used - for 4-bit ECC (EC4) [3:0] bits are used; [7:4] bits are floating
DQS[9:0]____A____t DQS[9:0]__B_t	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The Data Strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM supports differential Data Strobe only and does not support single-ended.
DQS[9:0]____A____c DQS[9:0]_B_c	
TDQS[9:5]____A____t TDQS[9:5]__B_t	Dummy load for matching the loading for mixed populations of x8 based RDIMMs and x4 based RDIMMs. Not used on LRDIMMs.
TDQS[9:5]____A____c TDQS[9:5]__B_c	
DLBDQ	Loopback Data output: The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled it is in driver mode using the default RON described in the Loopback Function section. When Loopback is Disabled the pin is either terminated or Hi-Z based on MR36: OP[2:0].
DLBDQS	Loopback Data Strobe output: This is a single ended strobe with the rising edged aligned with Loopback Data edge, falling edge aligned with Data center. When Loopback is enabled it is in driver mode using the default RON described in the Loopback function section. When Loopback is disabled, the pin is either terminated Or Hi-Z based on MR36: OP[2:0] .
RFU	Reserved for Future Use: No on DIMM electrical connection is present.
VIN BULK	External power supply: 12V, 4.25V (min), 15V (max)
VIN_MGMT	External power supply: 3.3V, 3.0V (min), 3.6V (max)
VSS	Ground

6. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on VDD supply relative to Vss	VDD	-0.3 ~ 1.4	V
Voltage on VDDQ pin relative to Vss	VDDQ	-0.3 ~ 1.4	V
Voltage on VPP pin relative to Vss	VPP	-0.3 ~ 2.1	V
Voltage on any pin relative to Vss	VIN, Vout	-0.3 ~ 1.4	V
Storage temperature	TSTG	-55 ~ +100	℃

Note: DDR5 SDRAM component specification.

DDR5 RDIMM PMIC DC Operating Voltage

symbol	Parameter	Voltage Rating (Volts)			Maximum Expected Current (Amps)	Power State
		Minimum	Typical	Maximum		
VIN_BULK	Host supply Voltage	4.25	12.0	15	2.5(maximum)	Operational
VIN_MGMT	Host supply Voltage	3.0	3.3	3.6	0.110(minimum)	Operational
VDD	PMIC Output supply Voltage	1.067	1.1	1.167	Note 1	Operational
VDDQ	PMIC Output supply Voltage	1.067	1.1	1.167	Note 1	Operational
VPP	PMIC Output supply Voltage	1.746	1.8	1.908	Note 1	Operational
1.8V LDO	PMIC Output supply Voltage	Note 2	1.8	Note 2	0.025(maximum)	Operational
1.0V LDO	PMIC Output supply Voltage	Note 2	1.0	Note 2	0.020(maximum)	Operational

Note1:DDR5 SDRAM component specification.
Note2:The VIN_MGMT supply is used to generate the internal bias voltage for reading operation from its internal nonvolatile memory content and to supply VLDO 1.8V& VLDO 1.0v. At power on, the VIN_MGMT supply shall reacha minimum of 2.8V before it can be detected as a valid input supply to the PMIC. The VIN_MGMT supply is strictlya voltage input.

Operation Temperature Condition

Parameter	Symbol	Value	Unit	Note
Normal Operating Temperature Range	TC	0~+85	℃	
Extended Temperature Range (Optional)	TC	+85~+95	℃	1

Note: (1) Refresh commands must be doubled in frequency, reducing the refresh interval tREFI to 3.9μs

7. DC Operating Condition

DC Operating Conditions

Symbol	Parameter	Low Freq Voltage Spec Freq: DC to 2MHz				Z(f) Spec Freq: 2Mhz to 10Mhz		Z(f) Spec Freq: 20Mhz		Notes
		Min.	Typ.	Max.	Unit	Zmax	Unit	Zmax	Unit	
VDD	Device Supply Voltage	1.067 (-3%)	1.1	1.166 (+6%)	V	10	mOhm	20	mOhm	1,2,3
VDDQ	Supply Voltage for I/O	1.067 (-3%)	1.1	1.166 (+6%)	V	10	mOhm	20	mOhm	1,2,3
VPP	Core Power Voltage	1.746 (-3%)	1.8	1.908 (+6%)	V	10	mOhm	20	mOhm	3

Note(s):

1. VDD must be within 66mv of VDDQ
2. AC parameters are measured with VDD and VDDQ tied together.
3. This includes all voltage noise from DC to 2 MHz at the DRAM package ball.
4. Z(f) is defined for all pins per voltage domain. Z(f) does not include the DRAM package and silicon die.

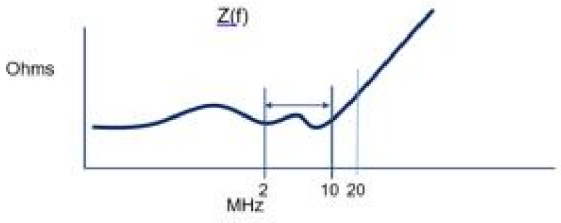


Figure 1 — Zprofile/Z(f) of the system at the DRAM package solder ball (without DRAM component)

A simplified electrical system load model for Z(F) with the general frequency response is shown in the figure below. The resistance and inductance can be scaled to generalize the spec response to the DRAM pin.

8. AC Characteristic

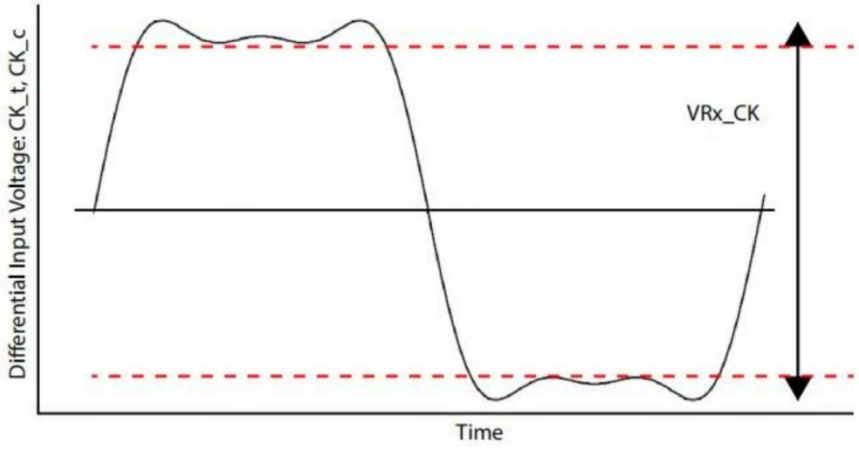
DRAM CA, CS Parametric values for DDR5-3200 to 4800

Parameter	Symbol	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Rx Mask voltage - p-p	VciVW	-	140	-	140	-	140	-	130	-	130	mV	1,2,4
Rx Timing Window	TcIVW	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	UI*	1,2,3,4, 8
CA Input Pulse Amplitude	VIHL_AC	160		160		160		150		150		mV	7
CA Input Pulse Width	TcIPW	0.58		0.58		0.58		0.58		0.58		UI*	5,8
Input Slew Rate over VcIVW	SRIN_cIVW	1	7	1	7	1	7	1	7	1	7	V/ns	6

Note(s):

1. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2. Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).
3. Rx differential CAto CK jitter total timing window at the VcIVW voltage levels.
4. Defined over the CA internal VREF range. The Rx mask at the pin must be within the internal VREFCA range irrespective of the input signal com- mon mode.
5. CA only minimum input pulse width defined at the Vcent_CA(pin mid).
6. Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).
7. VIHL_AC does not

Input AC & DC Logic Level for differential signals:



9. IDD Specification

Symbol	DDR5-5600 46-45-45 IDD Max. VDD 1.1V	Unit
IDD0	280.5	mA
IDDOF	364.9	mA
IDD2N	251.3	mA
IDD2NT	317.4	mA
IDD2P	151.1	mA
IDD3N	283.5	mA
IDD3P	162.7	mA
IDD4R	660	mA
IDD4W	776.5	mA
IDD5B	635.1	mA
IDD5C	389.6	mA
IDD5F	635.5	mA
IDD6N	44.0	mA
IDD7	1016	mA
IDD8	38.9	mA

10. Timing Measurement

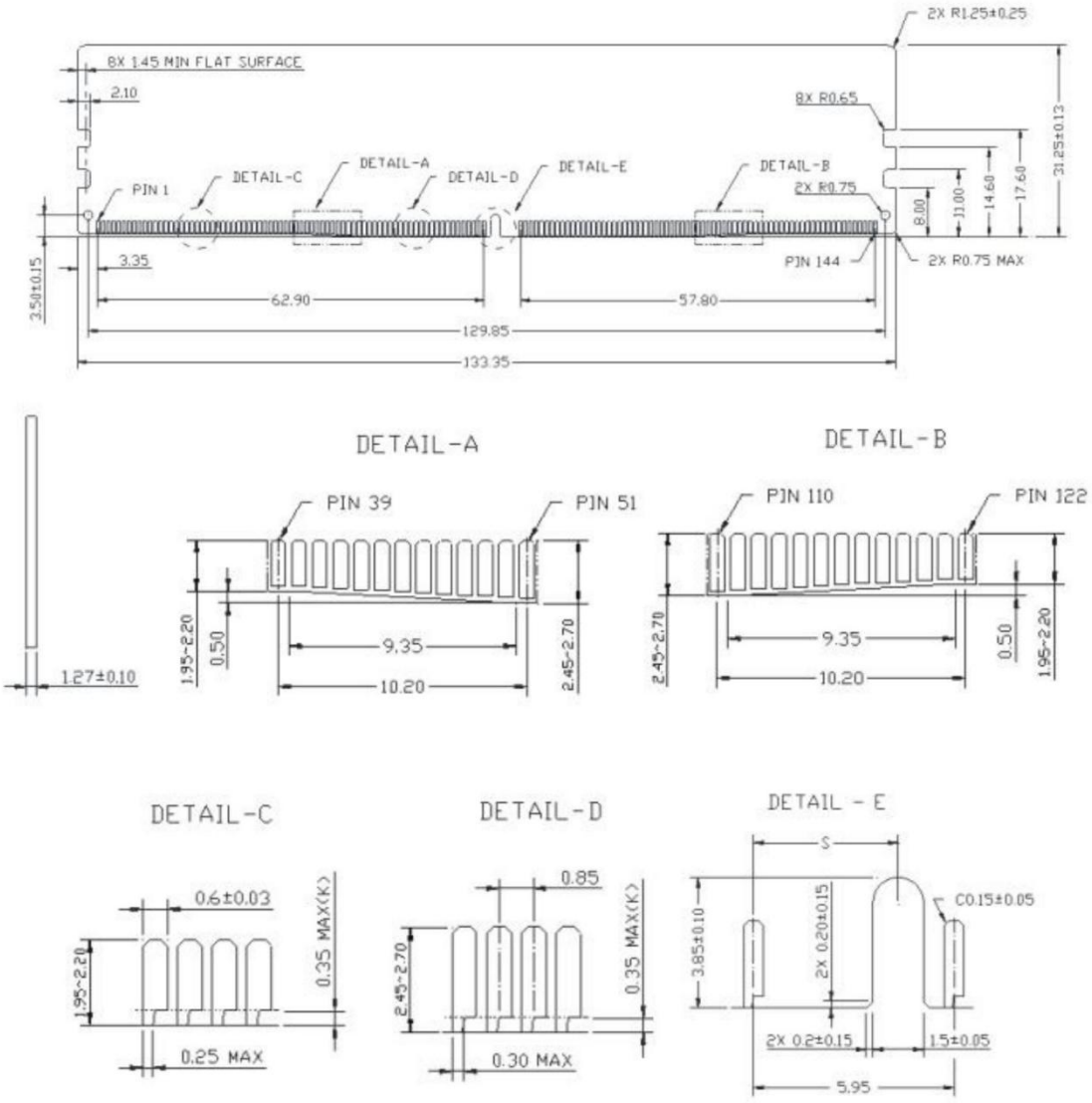
Speed Bin					DDR5 4400AN		DDR5-4400B		DDR5-4400BN		DDR5 4400C		Unit	NOTE
CL-nRCD-nRP					32-32-32		36-36-36		36-36-36		40-39-39			
Parameter				Symbol	min	max	min	max	min	max	min	Max		
Read command to first data				tAA	14.545	22.222	16.000	22.222	16.363	22.222	17.500	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.545	-	16.000	-	16.363	-	17.500	-	ns	7
Row Precharge Time				tRP	14.545	-	16.000	-	16.363	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.545	-	48.000	-	48.363	-	49.500	-	ns	7,8
CAS Write Latency				CWL	CL-2								nCK	
Speed Bins	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	RESERVED								ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED								ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	RESERVED		ns	
4400AN	14.545	14.545	32	tCK(AVG)	0.454	<0.500	RESERVED						ns	
Supported CL					22,24,26,28,30,32,36,40		22,26,28,30,32,36,40		22,28,30,32,36,40		22,28,32,36,40		nCK	

Speed Bin		DDR5-4800AN		DDR5-4800B		DDR5 4800BN		DDR5-4800C		Unit	NOTE
CL-nRCD-nRP		34-34-34		40-39-39		40-40-40		42-42 42			
Parameter	Symbol	min	max	min	max	min	max	min	Max		
Read command to first data	tAA	14.166	22.222	16.000	22.222	16.666	22.222	17.500	22.222	ns	12
Activate to Read or Write command delay time	tRCD	14.166	-	16.000	-	16.666	-	17.500	-	ns	7
Row Precharge Time	tRP	14.166	-	16.000	-	16.666	-	17.500	-	ns	7
Activate to Precharge command period	tRAS	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period	tRC (tRAS +tRP)	46.166	-	48.000	-	48.666	-	49.500	-	ns	7,8
CAS Write Latency	CWL	CL-2								nCK	

Speed Bin[5]	tAAmin (ns)[5]	tRCDmin tRPmin (ns)[5]	Read CL[12]	Supported Frequency Down Bins									
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED								ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	0.454	<0.500	RESERVED				ns	
4400AN	14.545	14.545	32	tCK(AVG)	0.454	<0.500	RESERVED						ns	
4800C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
4800B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
4800AN	14.166	14.166	34	tCK(AVG)	0.416	<0.454	RESERVED						ns	
Supported CL					22,24,26,28,30,32,34,36,40,42		22,26,28,30,32,36,40,42		22,28,30,32,36,40,42		22,28,32,36,40,42		nCK	

Speed Bin					DDR5-5600AN		DDR5-5600B		DDR5-5600BN		DDR5-5600C		Unit	NOTE
CL-nRCD-nRP					34-34-34		40-39-39		40-40-40		46-45-45			
Parameter				Symbol	min	max	min	max	min	max	min	Max		
Read command to first data				tAA	14.166	22.222	16.000	22.222	16.666	22.222	17.500	22.222	ns	12
Activate to Read or Write command delay time				tRCD	14.166	-	16.000	-	16.666	-	17.500	-	ns	7
Row Precharge Time				tRP	14.166	-	16.000	-	16.666	-	17.500	-	ns	7
Activate to Precharge command period				tRAS	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	32.000	5 x tREFI1	ns	7
Activate to Activate or Refresh command period				tRC (tRAS +tRP)	46.166	-	48.000	-	48.666	-	49.500	-	ns	7,8
CAS Write Latency				CWL	CL-2								nCK	
Speed Bins	tAAmin (ns)5	tRCDmin tRPmin (ns)5	Read CL12	Supported Frequency Down Bins										
-	20.952	-	22	tCK(AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	tCK(AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	tCK(AVG)	0.625	0.681	0.625	0.681	RESERVED				ns	
3200AN	15.000	15.000	24	tCK(AVG)	0.625	0.681	RESERVED						ns	
3600C	17.777	17.777	32	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	tCK(AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	RESERVED		ns	
3600AN	14.444	14.444	26	tCK(AVG)	0.555	<0.625	RESERVED						ns	
4000C	18.000	17.500	36	tCK(AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	tCK(AVG)	0.500	<0.555	0.500	<0.555	RESERVED				ns	
4000AN	14.000	14.000	28	tCK(AVG)	RESERVED								ns	
4400C	18.181	17.727	40	tCK(AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	tCK(AVG)	0.454	<0.500	0.454	<0.500	RESERVED				ns	
4400AN	14.545	14.545	32	tCK(AVG)	0.454	<0.500	RESERVED						ns	
5600C	17.500	17.500	42	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
5600BN	16.666	16.666	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	RESERVED		ns	
5600B	16.666	16.250	40	tCK(AVG)	0.416	<0.454	0.416	<0.454	RESERVED				ns	
5600AN	14.166	14.166	34	tCK(AVG)	0.416	<0.454	RESERVED						ns	
Supported CL					22,24,26,28,30,32,34,36,40,42		22,26,28,30,32,36,40,42		22,28,30,32,36,40,42		22,28,32,36,40,42		nCK	

11. Dimensions



12. Dimensions